Generic vs custom
Analogue vs digital

On the implementation of an online EEG signal processing algorithm

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Objectives

• We aim to:
  – Highlight the stringent power requirements of onboard EEG signal processing.
  – Estimate our ability to meet these requirements using different algorithm implementation techniques.
There is a trade-off between the flexibility, the power consumption and the circuit design techniques used.

[Werder, 2007]
Battery size

- Historically doubled every 5 – 20 years. [Wang and Chandrakasan, 2002]
- Approximate battery capacities: [Yates et al, 2007]

<table>
<thead>
<tr>
<th>Battery</th>
<th>Capacity</th>
<th>Volume / cm³</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>mAh</td>
<td>mWh</td>
</tr>
<tr>
<td>AA</td>
<td>2500</td>
<td>3500</td>
</tr>
<tr>
<td>Large coin cell</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>Small coin cell</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Target</td>
<td>N/A</td>
<td>100</td>
</tr>
</tbody>
</table>
Battery size in context

• Electrode, battery, electronics.
Online compression

- To reduce power consumption we aim to reduce the amount of data to be transmitted from the device.

- Can be implemented in the analogue or digital domain.
- Want to look at the power budget for compression to be beneficial.
Power budget

• System power without compression:

\[ P_{\text{Total}} = N P_{\text{amp}} + N P_{\text{ADC}} + J f_s R N \]

• System power with compression:

\[ P_{\text{Total}} = N P_{\text{amp}} + N P_{\text{ADC}} + P_c + C J f_s R N \]

• To be beneficial:

\[ P_c < J N f_s R (1 - C) \]
In practice

- Want to be an order of magnitude or so below this limit.

- Only seen one paper that gives EEG compression ratio and power consumption: [Avila et al, 2006]
  - $C = 0.02$ (98% compression)
  - $J = 5\text{nJ}/\text{bit}$, $N = 32$, $f_s = 200\text{ Hz}$, $R = 12\text{ bit}$.
  - Power budget = $376\text{ }\mu\text{W}$.
  - Used power = $72\text{ mW}$. 
Our algorithm

- Want to investigate how going to implement.
- Aim is discontinuous monitoring.
  - More details later in session.
- Targeting ~50% data reduction.
- Power budget 192 µW.
Processing steps

• Per channel:
  – 2: 7\textsuperscript{th} order (in the s domain) band pass filters.
  – 1: 2\textsuperscript{nd} order (in the s domain) low pass filter.
  – 2: Delay elements.
  – 1: Rectifier.
  – 2: Magnitude comparators (|a| > |b|?).
  – 1: Multiplier.
  – 1: Switch.

• Total of 10 processing steps.
Analogue implementation

- Based upon previous work in our research group.

- 2 band pass filters:
  - Experimental results of similar filter and work done so far: 200 nW.

- 1 low pass filter:
  - Simulated results, awaiting fabrication: 10 nW.

- 2 delay elements:
  - Work in progress, structures resemble filters: 200 nW.
Analogue implementation

- 1 rectifier:
  - Experimental results: 140 nW.
- 2 magnitude comparators:
  - Slight re-design required: 40 nW.
- 1 multiplier:
  - Structure resembles transconductor in filter: 100 nW.
- Switch:
  - Negligible.
Analogue total

- 700 nW per channel.
- For a 32 channel system: 23 µW.
  - 24% of power budget.
  - Nearly the order of magnitude below wanted.
- Large scope for errors in assumptions here.
  - Or for even longer lifetime systems.
Digital implementation

- Based upon lower bounds for the number of operations to be performed.

- 2 band pass filters:
  - In z domain 12 multiplications and 11 additions required: 46 operations per sample.

- 1 low pass filter:
  - In z domain: 7 operations per sample.

- 2 delay elements:
  - Store current value and retrieve previous one: 2 operations per sample.
Digital implementation

- 1 rectifier:
  - Remove a sign bit: 1 operation per sample.
- 2 magnitude comparators:
  - Remove sign bits and take comparison: 3 operations per sample.
- Multiplier:
  - 1 operation per sample.
- Switch:
  - 1 operation per sample.
Digital total

• 66 high level operations per sample.
• Preliminary implementation on TI C6000 series DSP took:
  – 1100 instructions, or 2000 cycles.

• Then need to operate on each sample and channel.
  – Estimate is 422 400 operations per second.
Digital total

- But 422 400 operations per second isn’t practical for 192 µW.
- Typical TI MSP 430 power consumption: [TI, 2007]

<table>
<thead>
<tr>
<th>Clock speed / kHz</th>
<th>Power consumption / µW</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>594</td>
</tr>
<tr>
<td>100</td>
<td>132</td>
</tr>
<tr>
<td>4</td>
<td>11</td>
</tr>
</tbody>
</table>

- Insufficient clock cycles are available.

- [Catthoor, 2004] estimates the performance of a fully custom digital circuit as 1 µW/MIPS.
  - Algorithm should be workable with this performance.
Comparison

- Custom analogue: Achievable within power budget.
- Generic digital: Not achievable.
- Custom digital: Should be achievable.

- Custom solutions give better performance, and need this if systems are to be realisable.

- Given this, we are pursuing the custom analogue approach.
Summary

✓ Battery size for miniaturization severely limits the power available for onboard signal processing.

✓ The power budget is ideally of the order of 10’s of µW.

✓ Generic approaches do not meet this.
✓ Preliminary work indicates that a custom analogue solution does meet it while a custom digital should.

✓ As such we are pursuing the custom analogue approach.