Switched Current Techniques

Prof. Chris Toumazou
A very brief note on the Switched Current (SI) technique

Analogue signal processing has been dominated over the last decade by the SC filter technique. Unfortunately SC filters have never really fitted in with standard VLSI processing generally because of their requirement for a linear floating capacitor (double poly-silicon) leading to special process options which can be very expensive for a part that occupies maybe only 10-20% of a mixed-mode ASIC chip. The SC technique will undoubtedly suffer in a decade where we are witnessing tremendous changes in VLSI technology. Device technology is being optimised for digital performance, power supply voltages are reducing, threshold voltages are getting smaller, logic gate leakage will be more dominant preventing optimum SC filter performance. There is a limited headroom to operate high gain op-amps, analogue switch performance will be limited due to suboptimal threshold voltages and the extra processing for floating capacitors is unattractive. What do we do? As always operate in the current domain. A new powerful technique is the Switched Current (SI) technique. Linear floating capacitors are not necessary, voltage swings are small due to current domain operation and the technique requires no op-amps. The technique fully exploits VLSI technology and we will explain it here with a brief example of a SI current-mirror (dynamic mirror) and a lossless SI integrator. It must be emphasised at the outset that the ultimate limitation of the SI technique on accuracy will be charge injection and noise due to the switches limiting dynamic range (resolution)
A few home truths about analog...........

• Egg is getting bigger, Shell is getting smaller

• Major role of analog signal processing interfacing DSPs to outside world

• Competitive Consumer electronics market - low cost

Solutions

Trade analog process technology for cheap digital process VLSI technology

Analog precision for digital precision

How?
Switched-Currents to the rescue.............

DIGITAL TECHNOLOGY

J₁

iᵢₙ(z) φ₁

BASIC CELLS

FILTERS

DATA CONVERTERS

Analogue

Digital

J₂

φ₂ iₒᵤ(z)

FUTURE DIRECTIONS

ANALYSIS AND TEST

OTHER APPLICATIONS

SWITCHED-CURRENTS

- Fully Compatible with digital processing
- Current domain operation gives low supply voltage potential
- No opamps required
- High speed potential
- Utilises SC techniques directly

So what's the trick.............?
1. Motivation

- Emergence of complete single chip mixed-mode signal processing systems.

- Need to include analogue interface circuits on a primarily digital chip.

- Analogue circuits should be fully compatible with digital processing technology

- Traditionally switched-capacitors (SC's) used for analogue interfacing

- SC's require a linear capacitor

- Reduced supply voltages degrade SC performance.

- A new technique that is fully compatible with digital processing is needed.
Switched-Currents are a viable alternative to Switched-Capacitors because:

- Fully compatible with digital processing technology

- Current domain operation gives low supply voltage potential

- No operational amplifiers required

- High speed potential

- Utilises SC design techniques directly
2. Basic Cells

Basic Idea - An MOS transistor requires no gate current to maintain its drain-source current.

(i) First generation

Track-and-hold memory cells

![Diagrams](image)

(a) Uni-directional currents
(b) Bi-directional currents

- Implements a current track-and-hold element
- A linear capacitor is not required, $C_{gs}$ is used
- Accuracy depends on matching of $M_1$ and $M_2$
- Has poor sensitivity properties when used to realise an integrator
Second generation SI cell

**BASIC OPERATION OF SI CELL**

![Circuit Diagram](image)

**SEPERATE PHASES**

φ₁  φ₂

**SAMPLE**

**HOLD**

Diode Connected

Current Sink
(ii) Second Generation

Sample-and-hold memory cell

(a) Circuit structure
(b) Clock waveforms

- The need for matching is eliminated
- A linear capacitor is not required, the $C_{gs}$ of $M_1$ is used
- Implements $\frac{i_o}{i_{in}}(z) = -z^{-1/2}$
- A continuous scaled output can be added
3. Building Blocks

(i) Delay cell

- Consists of alternately clocked memory cells
- Implements \( \frac{i_o}{i_{in}} (z) = z^{-1} \)

A delay cell was integrated to verify the principle

**Observed output**

\[ X = 200 \mu s/\text{div} \]
\[ Y = 20 \mu A/\text{div} \]

Clock frequency 10kHz, input 1kHz
Upper trace input, lower trace output
(ii) Ideal integrator

During $\phi_2(n-1)$

\[ i_{d2}(n-1) = 2J + i_{in}(n-1) - i_{d1}(n-1) \]

\[ = J + i_{in}(n-1) + \frac{i_o(n-1)}{A} \]

During $\phi_1(n)$

\[ i_{d1}(n) = J - i_{in}(n-1) - \frac{i_o(n-1)}{A} \]

\[ i_o(n) = Ai_{in}(n-1) + i_o(n-1) \]

Since $Z = C_sT$  \[ \Rightarrow \frac{i_o(z)}{i_{in}} = \frac{Az^{-1}}{1 - z^{-1}} \]

When $(L_0/Lw) \approx \frac{1}{S(T/A)} \Rightarrow \omega T \ll 1$

The switched-current integrator

- requires no op-amps
- requires no linear capacitors
- can operate on reduced supply voltages
Example of 'Switched Current Integrator'

On phase $\phi_2$ of clock period $(n-1)$

$I_{2}(n-1) = 2I_{B} + I_{1}(n-1) - I_{1}(n-1)$

where

$I_{1}(n-1) = \frac{A I_{B} - I_{0}(n-1)}{A} = I_{B} - \frac{I_{0}(n-1)}{A}$

$\therefore I_{2}(n-1) = I_{B} + I_{1}(n-1) + \frac{I_{0}(n-1)}{A}$

On phase $\phi_1$ of clock period $(n)$

$I_{1}(n) = 2I_{B} - I_{2}(n-1)$

$= I_{B} - I_{1}(n-1) - \frac{I_{0}(n-1)}{A}$

or

$A I_{1}(n) = A I_{B} - A I_{1}(n-1) - I_{0}(n-1)$

Now $A I_{B} - A I_{1}(n) = I_{0}(n)$

$\therefore I_{0}(n-1) + I_{0}(n-1) = I_{0}(n)$

Taking $Z$ transforms gives

$H(z) = \left(\frac{I_{0}(n)}{I_{1}(n)}\right) z = \frac{A z^{-1}}{(1 - z^{-1})}$
$$\begin{align*}
\therefore \quad H(\omega) &= \frac{A}{Z' - 1} \\
Z' &= (1 + j\omega T) \quad \text{assumes } \omega T \ll 1 \\
\text{where } \omega T \text{ is clock period}
\end{align*}$$

$$\begin{align*}
\therefore \quad H(\omega) &\approx \left[ \frac{1}{j\omega T A} \right] \quad \text{lossless integrator} \\
\text{Time constant } \tau &= \frac{T}{A} = \frac{1}{f_c A}
\end{align*}$$

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Book reference

'Analogue IC Design: The Current-mode approach'
(Chapter 11), Eds. C. Toumazou, F.J. Liogey
and O. G. Haigh.
Verification of integrator

- Fabricated using a 1.6μm process.
- Regulated cascode memory transistors used.

Measured waveforms

![Waveform Image]

- 10kHz clock
- 1kHz input
- X = 200μs/div
- Y = 20μA/div

Measured frequency response

![Frequency Response Graph]

- Clock frequency 100kHz
4. Limitations

(i) Drain voltage variations
(ii) Charge injection
(iii) Settling
(iv) Noise
(v) Signal swing
(vi) Mismatch
(i) Drain voltage variations

- $V_{ds1}$ different during $\phi_1$ and $\phi_2$

- Error due to capacitive gate-drain coupling

- Conductance ratio error

  Finite output conductance $g_o$

  Finite input conductance $g_m$

- Similar to the effect of finite gain op amp in SC
Output conductance reduction techniques

Simple Cell

\[ R_o = r_{ds1} \]

Cascoded Cell

\[ R_o = g_{m2}r_{ds1}r_{ds2} \]

Regulated Cascode Cell

\[ R_o = g_{m2}g_{m3}r_{ds1}r_{ds2}r_{ds3} \]
Operation of the Regulated Cascode Cell

![Circuit Diagram]

\[ J = 100 \mu A \]
\[ I_B = 5 \mu A \]

**M₁ Saturated**

\[ M₁ = 100/20 \mu m \]
\[ M₂, M₃ = 100/2 \mu m \]
\[ g_{m₁} \propto \sqrt{I_{ds₁}} \]
\[ \frac{C}{g_{m₁}} = 11.3 \text{ns (at 100 \mu A)} \]
\[ R_o \approx 10 \text{G\Omega} \]
\[ V_{o(min)} = 1.2 \text{V} \]

**M₁ Nonsaturated**

\[ M₁ = 25/20 \mu m \]
\[ M₂, M₃ = 100/2 \mu m \]
\[ g_{m₁} \equiv \text{constant} \]
\[ \frac{C}{g_{m₁}} = 10.4 \text{ns} \]
\[ R_o \approx 80 \text{M\Omega} \]
\[ V_{o(min)} = 1.05 \text{V} \]
(ii) Charge injection

- Error in memorised gate voltage caused by charge injected from the diode-connecting switch transistor

Simple switch model

- Causes gain error and harmonic distortion
- Similar to charge injection in SCs
- Negative feedback reduces error
Simple switch  Dummy switch compensation

- Needs good matching and clock accuracy

- Fully differential structures effective at rejecting charge injection errors

Algorithmic Cell

Circuit structure

Clock waveforms

<table>
<thead>
<tr>
<th>Period</th>
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<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi_1$</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>$\phi_2$</td>
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<tr>
<td>$\phi_3$</td>
<td></td>
<td></td>
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<tr>
<td>$\phi_4$</td>
<td></td>
<td></td>
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<tr>
<td>$\phi_5$</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>
(iv) Noise

- Noise is generated by the MOS transistors.
- Both 1/f and thermal noise are produced.
- Correlated Double Sampling (CDS) reduces the effect of 1/f noise.
- The sampling operation alters the shape of the noise.
- Both sampled and direct (nonsampled) noise are present at the output.

Measured noise in a S/H cell
Measured noise in an ideal integrator

- Noise in the S/H cell is shaped by the sinc function of the cell.
- Noise in the integrator is integrated.
- Undersampled wideband thermal noise dominates.
- The noise performance of the integrator is a major limitation to the performance of filters based on it.
3(iii) Signal swing

- Signal swing improved using class AB techniques.

Class A memory cell

Class AB memory cell

Simulated results

- Class AB cell uses one tenth the bias current to achieve the same signal swing.
(iii) Settling

(a) Circuit diagram

(b) Small signal model

- Small signal transfer function

\[ H(s) = -\frac{1}{1 + s\left[\frac{C + C_d}{g_m}\right] + s^2\left[\frac{C C_d}{g_m g_s}\right]} \]

- Introduces parasitic integrator

- Effect similar to unity gain bandwidth in SC
S\textsuperscript{2}I SWITCHED-CURRENT MEMORY CELL

REFERENCE
OPERATION OF $S^2$I CELL

1. Sample and hold the input current $i$ approximately in the coarse memory C
2. Derive the error in memory C and store the error in memory F

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**Phase 1a**

- $V_{dd}$
- $V_{ref}$
- $i$ to $M2$ to $J$
- $M1$ to $J+i$
- $V_{dd}$

**Phase 1b**

- $V_{dd}$
- $V_{ref}$
- $i$ to $M2$ to $J+\delta_i$
- $M1$ to $J+i+\delta_i$
- $V_{dd}$

**Phase 2**

- $V_{dd}$
- $M2$ to $J+\delta_i+\Delta_i$
- $i-\Delta_i$ to $M1$
- $M1$ to $J+i-\delta_i$
- $V_{dd}$

**Clock scheme**

- $\phi_1$
- $\phi_{1a}$
- $\phi_{1b}$
- $\phi_2$

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Page 26 of 45
CMOS class A $S^{n}l$ cell with three stages shown

During $\phi_2$, the output current from the respective stage is

\[ i_c = i_{in} - \delta_1 \quad i_{f1} = \delta_1 - \delta_2 \quad i_{f2} = \delta_2 - \delta_3 \]

The output current is the combination of the three and equals

\[ i_o = i_c + i_{f1} + i_{f2} = i_{in} - \delta_3 \]

where $\delta_3$ is an second order error.

REFERENCE
COMPARISON OF TRANSMISSION ERROR BETWEEN
A TWO- AND A THREE-STAGE S\textsuperscript{n}I CELL

REFERENCE
C. Toumazou and S. Xiao: ‘n-step charge injection cancellation scheme for very
Class AB S2I Memory Cell

\[ \phi_{11} \]

\[ \phi_{12} \]

\[ \phi_2 \]
Equivalent SC integrator

(a) Circuit structure

(b) Signal flowgraph representation

- Has the same transfer function as the generalised switched-current integrator
- Sensitivity to ratio errors is the same
- Switched-current integrator can be used as direct replacement in filter designs
Generalised integrator

(a) Circuit structure

(b) Signal flowgraph representation

\[
 i_o(z) = \frac{A_1 z^{-1}}{1 - B z^{-1}} i_1(z) - \frac{A_2}{1 - B z^{-1}} i_2(z) - \frac{A_3 (1 - z^{-1})}{1 - B z^{-1}} i_3(z)
\]

where

\[
 A_1 = \frac{\alpha_1}{1 + \alpha_4}, \quad A_2 = \frac{\alpha_2}{1 + \alpha_4}, \quad A_3 = \frac{\alpha_3}{1 + \alpha_4}, \quad B = \frac{1}{1 + \alpha_4}
\]

- Can be used as a bilinear integrator if
  \[ i_1 = i_2 = i, \; i_3 = 0 \] and \[ \alpha_1 = \alpha_2 = \alpha, \; \alpha_3 = 0 \]
Generalised Class AB integrator

- Implements exactly the same transfer function as the equivalent class A integrator.
- Requires only one bias chain.
- Overall power saving compared to class A ≈ an order of magnitude.
5. Filter Synthesis

- Switched-currents realise the same functions as SCs
- Switched-capacitor design techniques used directly
- Three classical filter types
  - FIR
  - Biquad
  - Ladder

(also wave active filters)

(i) Finite impulse response (FIR)

![Diagram of FIR filter]

- Well suited to switched-currents
- Uses a cascade of delay cells
- Coefficients realised as scaled mirrors
(iii) Ladder Filters

- Uses the same design techniques as switched-capacitors

- Design Procedure
  
  (i) Choose passive prototype to meet specification
  
  (ii) Prewarp filter
  
  (iii) Convert prototype to s-domain SFG
  
  (iv) Map SFG into z-domain
  
  (v) Implement using switched-current integrators

Passive Prototype
Signal flow graph in the s-domain

Signal flow graph in the z-domain
6. Elliptic Filter Example

Design Targets

\[ f_c = 0.18f_{\text{clock}} \]
\[ f_a = 0.22f_{\text{clock}} \]
Ripple < 0.4dB
Min Atten > 25dB
Clock rate ≈ 20MHz

Filter Details

Fifth order elliptic filter chosen

Implemented on a 1.2\( \mu \)m n-well CMOS process

Uses class A regulated cascode memory cells

Does not use dummy switches

Area 1.4 sq mm (not optimised)

Layout not optimised for matching
Photograph of chip
Measured results - 2MHz clock

Ref-9 (dBm) 5 (dB/div) Range (dBm) 10 Marker: 100000 (Hz) at -13.35 (dBm)

Start 100000 (Hz) RBW 3 KHZ VBW 100 HZ ST 9.4 SEC Stop 1.E+6 (Hz)
7. Data Converter Applications

- Switched-currents are well suited to application in a range of current mode data converters

- They have already found several uses:
  
  Self-calibrating D/A converters
  
  Algorithmic A/D converters
  
  Sigma-delta modulators

- Sigma-delta modulators are particularly promising
So what is the fundamental limit on dynamic range and resolution in a sampled data converter?

Advances in design techniques such as the current-mode algorithmic converter are a necessary part of the evolution of analogue IC design. In many signal processing applications, the need for high precision or large dynamic range is increasing. For example, stereo audio requires analogue-digital converters approaching 16-bit accuracy with bandwidths up to 20-40kHz. 16-bits corresponds to a dynamic range of 96 dB which is extremely difficult to achieve even in present technology. Other problems occur when switches are used. Switches inject a noise called kT/C. This noise is inherent in any circuit which charges a capacitor through a switch. This relationship will be developed as an example of the problems facing the analogue designer. Assume that the maximum clock frequency of the switch is \( f_c \) and is given as

\[
f_c = \frac{1}{t_s} = \frac{1}{10RC}
\]

where \( t_s \) is the settling time caused by the resistance of the switch (R) and the capacitor (C) being charged (or discharged). The dynamic range, DR, can be defined as the ratio of the reference voltage, \( V_{\text{ref}} \), to the rms value of the kT/C noise and is expressed as

\[
DR = \frac{V_{\text{ref}}}{\text{Noise}} = \frac{V_{\text{ref}}}{\sqrt{kT/C}} = 2^N
\]

where \( N \) is the number of bits required. Solving for \( C \)

\[
DR = 2^N = \frac{V_{\text{ref}}}{\text{Noise}} = \frac{V_{\text{ref}}}{\sqrt{kT \cdot 10Rf_c}}
\]

Graphs of resolution for several values of \( V_{\text{ref}} \) and switch resistances are shown below. It is assumed that \( V_{\text{ref}} \) is equal to or less than the power supply. It is clear that the fundamental limit of the precision (bits) of sampled systems reduces as the sampling rate increases and as the power supply decreases. At a sampling rate of 10MHz, a reference voltage of 5V, and a switch resistance of 10kΩ, the precision is limited to 14 bits assuming all else is ideal. Fundamental limits such as kT/C noise will place a severe challenge on the creativity of analogue designers.
Relationship between resolution, sampling rate, and kT/C noise.

COURTESY Of Prof Phil Allen (Chapter 18 of Analogue IC Design: the current-mode approach, eds C. Toumazou F J Lidgey and D G Haigh, Peter Peregrinus, London 1990)

So what next......................... ???

Probably the most popular data conversion techniques for the 90s will no doubt be the sigma delta oversampling technique which trades analogue precision for digital precision. The technique offers probably the highest precision analogue-digital converter technique available today for reasons we will now discuss.
Sigma-Delta ADC

- Analogue signal sampled at a much higher rate than the desired output rate, allowing a simpler (slower roll-off) anti-aliasing filter
- Single-bit quantiser and DAC is sufficient for high resolutions - the ADC does not need accurately matched components
Analysis of Sigma-Delta Modulator

\[ Y(s) = E(s)H(s) + N(s) \]
\[ = [X(s) - Y(s)]H(s) + N(s) \]
\[ Y(s)[1 + H(s)] = H(s)X(s) + N(s) \]

\[ \therefore Y(s) = \frac{H(s)X(s) + N(s)}{1 + H(s)} \]

\[ \text{STF} = \frac{\partial Y(s)}{\partial X(s)} = \frac{H(s)}{1 + H(s)} \]

\[ \text{NTF} = \frac{\partial Y(s)}{\partial N(s)} = \frac{1}{1 + H(s)} \]

Input signal is unchanged but quantisation noise is shaped by the filter

**Accuracy Enhancement for High-Speed ADCs and DACs**
Noise-shaping in Sigma-Delta ADC

- Noise shaping moves quantisation noise from low frequencies to high frequencies.
- This effect is more pronounced for higher order modulators, allowing a lower oversampling ratio.
- The noise outside the signal band is then removed by the digital low-pass filter.
- Not used for high-speed A/D conversion.
Suggested problems – Current mirrors and switched currents

1. Calculate the frequency dependence of the input impedance of a source degenerated common source amplifier. Use this result to calculate the frequency dependence of the small signal input impedance of the Wilson current mirror. It may help to do the analysis as feedback problem rather than a circuit problem. Please remember the current input is meant to be driven by a vanishing admittance current source!

2. Calculate the DC current gain error for matched BJT transistors for the simple current mirror. Include the Early Effect. Use this result to infer the small signal current gain error of the MOS simple current at a finite frequency, if you know the $f_t$ of the process. Remember the finite frequency current gain of a MOS transistor is imaginary, i.e. incurs a 90 degree phase lag.

3. Calculate symbolically the small signal power gain of a simple BJT mirror at a finite frequency.

4. Calculate the harmonic distortion of a class A FET simple current mirror if the AC signal amplitude is equal to the bias, and if the AC signal amplitude is half the bias, both at a finite frequency. Note that in strong inversion the gate-source capacitance is essentially constant, so that the circuit IS NOT linear-time invariant!

5. Calculate symbolically and plot the I-V characteristic of a diode connected (gate-drain connected together) FET, for:
   a. A long gate FET: $I_{DS} = K_L \frac{W}{2L}(V_{GS} - V_T)^2 \left(1 - \lambda V_{DS}\right)$
   b. A short gate FET: $I_{DS} = K_S \frac{W}{1.5L}(V_{GS} - V_T - \alpha V_{DS})^{1.5}$
   c. In weak inversion: $I_{DS} = M \frac{W}{L} e^{\theta(V_{GS} - V_T)/kT} \left(1 - e^{\theta V_{DS}/kT}\right)$

For the purposes of this exercise you may assume $K_L = 10 \mu A/V^2$, $K_S = 10 \mu A/V^{1.5}$, $M = 100 nA$, $V_T = 0.3 V$, $\lambda = .01$ and $\alpha = .05$. What is the gm of each case? What are the typical impedance levels encountered?

6. Observe that a second generation switched current memory cell is equivalent to a simple current mirror driven by the signal masked by the switching waveform. Use the results form Q3 above, the Convolution theorem and Power conservation to estimate the gain error as a function of switching and signal frequency, provided the signal frequency satisfies the Nyquist criterion.