CCDF AND MONTE CARLO ANALYSIS OF A DIGITAL POLAR TRANSMITTER FOR ULTRA-WIDEBAND SYSTEM

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ABSTRACT

Polar modulation has been adopted by modern wireless systems due to its high power efficiency. In this paper, a novel behavioral model for a digital polar transmitter is presented. The polar transmitter contains an array of amplifiers, which are controlled digitally. A system level simulator is used to model each amplifier. The effects of different number of stages on the mandatory data rates are studied with respect to the error vector magnitude, in conformance to the ultra-wideband standard. Next the complementary cumulative distribution function is studied for a four-stage digital polar transmitter in order to gain an understanding of when each individual stage is turned on. Lastly, nonlinearity, modeled as gain variation for the different parallel stages, is included for a four-stage digital polar transmitter when the data rate is 480 Mbps. Results demonstrate the feasibility of obtaining high efficiency using digital polar transmitters for Multiband OFDM UWB systems.

I INTRODUCTION

Modern wireless communications have adopted signal types that provide high bandwidth efficiency. However, the high efficiency usually requires amplitude variations of the phase modulated Radio Frequency (RF) carrier. The Multiband OFDM Alliance (MBOA) standard for ultra-wideband (UWB) communication is one such wireless system [1]. These systems typically require a linear power amplifier (PA) to avoid out-of-channel interference and distortion. However, the power efficiency of a front end RF PA drops as the input power is backed off to the linear region. This leads to shorter battery lifetime.

The problem of low efficiency can be mitigated by using a polar transmitter [2]. In a polar transmitter, the amplitude and phase information are generated digitally from the cartesian representations of the signal. The digital phase information goes into a frequency synthesizer, which generates a RF signal, and drives the input of a nonlinear, high efficiency PA (usually a switch mode power amplifier), while the amplitude modulation is recombined by modulating the power supply of the PA.

In addition, the advancement of deep sub-micron semiconductor technology led to smaller devices which favour more digital circuits and control for radio system on chip [3].

A polar transmitter, based on a digitally-controlled PA, has been reported in the recent years [3, 4]. This digitally controlled polar transmitter architecture, shown in Fig. 1, has been adopted for narrowband wireless applications, like Bluetooth [3] and GSM/EDGE [4].

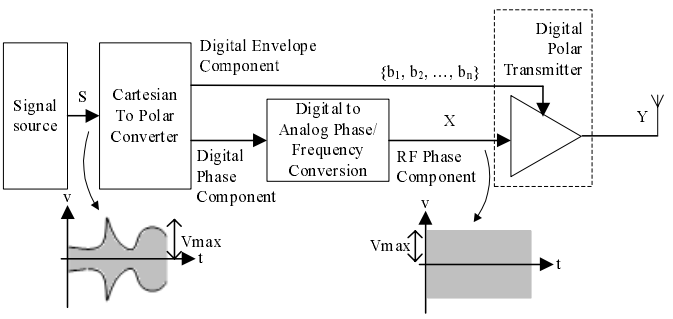

Figure 1: Block diagram of the polar transmitter architecture [3].

In this paper, the concept of a digital polar transmitter (DPT) model [3] is explored for UWB Mode 1 multiband OFDM applications. The DPT has been modelled and simulated in Agilent Advanced Design System (ADS), together with the UWB RF signal, the complementary cumulative distribution function (CCDF) and the error vector magnitude (EVM) measurement models found in [5], which are in conformance to [1]. Simulation results show the potential for a fully digital transmitter architecture for UWB.

Details of the proposed digital polar transmitter model are introduced in Section II. Simulations and results for the model are shown in Section III. Conclusions are given in Section IV.

II DIGITAL POLAR TRANSMITTER MODEL

Fig. 2 shows our proposed digital polar transmitter (DPT) architecture model for UWB, which was first reported in [6]. The polar transmitter consists of an array of parallel amplifiers[1], with each amplifier providing binary-weighted amplification. The digital envelope components, $\{b_1, b_2, ..., b_n\}$, are used to control the turning on/off of each amplifier. The b_1 bit controls the most significant bit (MSB) amplifier and b_n the least significant bit (LSB) amplifier, where n represents the resolution (the number of amplifiers). For example, for a resolution of 4 parallel stages, $\{b_1, b_2, b_3, b_4\} = \{1000\}$ implies that only the MSB amplifier is turned on. Hence, for this architecture, the

[1]Electrically, a choice is available on whether to operate the amplifiers in the voltage or current mode.

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need for digital-to-analog converters at the envelope output of the Cartesian-to-Polar converter is not required, and the control of the array of amplifiers is fully digital. The RF phase-

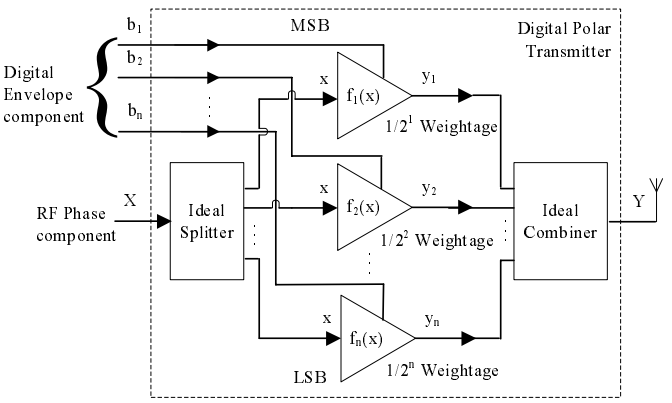

Figure 2: Proposed digital polar transmitter consisting of parallel array of amplifiers.

modulated signal, X, is applied at the input of the DPT, as shown in Fig. 1. X must be scaled to the maximum value of the signal at the output of the signal source, S, as the peak amplitude information is not reflected in the digital representation of the envelope component.

The concept of parallel amplification, reported in [7], results in low current levels in each individual amplifier, compared to the case of a single amplifier. The lower current levels in each branch implies that the requirement on the individual device sizes can be relaxed. As shown in Fig. 2, this is modelled with an ideal splitter in the ADS Ptolemy environment, where the input power to each individual amplifier becomes $x = X/n$. After the amplification stage, the signals for all the branches are combined with an ideal combiner. The output of the DPT is given by:

$$\begin{aligned} Y &= \sum_{i=1}^{n} y_i \\ &= \sum_{i=1}^{n} b_i f_i(x), \end{aligned} \tag{1}$$

where $f_i(x)$ is the input-output amplitude relationship of the i-th amplifier; b_i is the binary control to turn the i-th amplifier on/off; and y_i is the output of the i-th amplifier.

A Amplifier Model

In general, a Taylor polynomial expression can be used to model the input-output amplitude relationship of a typical nonlinear amplifier. This is given by:

$$y = a_0 + a_1 x - a_2 x^2 - a_3 x^3 + \ldots,\ a_i > 0, \tag{2}$$

where a_0 is a constant offset voltage, a_1 is the desired linear gain, and the negative terms model the undesired compressive behaviour of power amplifiers. In general, (2) is only valid over a certain range on the input and it does not converge when the input approaches infinity. Hence, there is a need to clamp the polynomial at critical points, such that the slope of the transfer curve goes to zero. Here, (2) can be modified as

$$y' = \begin{cases} a_0 + a_1 x - a_2 x^2 + \ldots, & \text{if } |x| \leq \text{critical value} \\ \pm y_{critical}, & \text{otherwise.} \end{cases} \tag{3}$$

The model for each amplifier within the DPT is based on (3), given by:

$$f_i(x) = \frac{1}{2^i} \times n \times y'. \tag{4}$$

Equation (4) includes two additional scaling factors: the factor $\frac{1}{2^i}$, which implements the binary-weighted amplification for the different amplifiers; and the factor n models the power splitter at the input of the DPT.

III Simulations and Results

The results are obtained based on computer simulations according to MBOA standard. This operates from 3.1 GHz to 10.6 GHz spectrum and divided into 14 bands of 528 MHz bandwidth, each band employs orthogonal frequency division multiplexing (OFDM) and PSK (Phase Shift Keying) to transmit data up to 480 Mbps. Initial results are derived from signal source centred at 3.960 GHz (Band 2) transmitting 480 Mbps which employs OFDM with QPSK with coding conforming to the fixed frequency interleaving (FFI) scheme, with time frequency code number of 6 for Band Group 1 [8].

The test signal is generated using a 511-bit pseudo-random pattern, and it is applied to an ideal Cartesian-to-Polar converter, to generate the envelope and phase information. The envelope information is used to control the parallel amplifiers in the DPT, while the phase information passes through a digital-to-analog phase and frequency conversion block to drive each parallel amplifier within the DPT (Fig. 1). Each parallel amplifier is modelled by an ADS amplifier model with gain compression. The power of the signal source is adjusted so that the output power density of the transmitter, assuming a 0-dBi gain antenna, does not exceed the FCC power spectral density (PSD) limit of -41.3 dBm/MHz. Based on the PSD limit, the transmit power cannot exceed -14.31 dBm. In the case where the linear gain a_1 = 10 dB, the input power limit of the signal source is -24.31 dBm.

The ADS simulator represents the envelope signal with a certain amplitude resolution. However, the amplitude resolution required for the DPT is n. Hence, in the simulation, we need to change the resolution of the envelope signal to n. At the same time, the envelope amplitude needs to be quantized to n bits.

A Resolution for different data rates

First, the result is simulated for a linear DPT ($f_i(x) = x \times \frac{1}{2^i} \times n \times a_1$), with different resolutions. This is to determine the minimum number of parallel amplifiers necessary to meet the requirement of EVM $<$ -19.5 dB [8]. The simulation is performed for each of the mandatory data rates (53.3 Mbps, 106.7 Mbps, and 200 Mbps) and the highest data rate (480 Mbps). In this case, the input power to the DPT is set

Table 1: Peak Values of the envelope signal for different data rates, when the input power is set to -24.31 dBm.

Data Rate (Mbps)	Peak Value (V)
53.3	0.077
106.7	0.060
200	0.056
480	0.062

to -24.31 dBm, and the peak value for the different data rates are shown in Table 1.

The results are shown in Fig. 3. Few observations can be made. First, a minimum resolution of 4 parallel amplifier stages is needed to fulfill the EVM requirement for all the data rates. Next, the EVM (for the different mandatory data rates) improves for decreasing peak value when a DPT uses fewer parallel stages (i.e. 3 and 4 stages). This is likely to be caused by higher quantization errors associated with a signal having a higher peak value. Lastly, as the number of parallel stages increases, the EVM is lower for decreasing mandatory data rates. However, the trend for the EVM result for data rate 480 Mbps does not seem to be consistent with the mandatory data rates. This could be due to the different time spreading factors and coding rates been used for the different data rates [1].

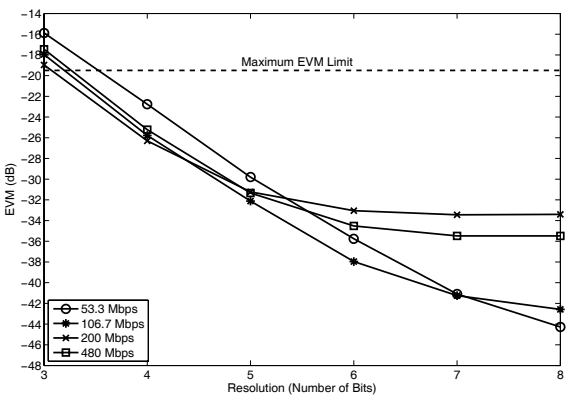

Figure 3: The effects of the number of stages, for different data rates, on EVM.

Next, 1-dB gain compression is introduced for each parallel amplifier (based on (4)) for different resolutions. Each parallel stage is modelled with the same input 1-dB gain compression power (P_{1dbcp}). As the P_{1dbcp} for each parallel amplifier (for different resolutions) is varied, the EVM remains constant, proving the fact that the linearity of an amplifier has no impact on a constant envelope signal.

B Complementary Cumulative Distribution Function and Power Efficiency

The peak-to-average power ratio (PAR) of the OFDM signal is typically characterized by its CCDF. The CCDF allows us to obtain the probability density function (PDF), which in turn be used to calculate the percentage of time each amplifier in a

Figure 4: CCDF simulation result for 480 Mbps, when the input power = -24.31 dBm. The horizontal axis variable, SignalRange_dB = absolute signal power - mean power.

DPT is turned on. The simulated CCDF is plotted in Fig. 4. In this case, the input power for the test signal generated using a 511-bit pseudo-random pattern is adjusted to -24.31 dBm. The corresponding mean power and the peak power are found to be -24.545 dBm and -16.056 dBm respectively. The PDF can be obtained based on Table 3. Based on the PDF results obtained, the percentage of time when each parallel amplifier is found to be turned on, is shown in Table 2.

Table 2: Percentage of time when each bit is turned on (480 Mbps).

Bit	Percentage of turn on time (%)
b_1 (MSB)	7.5
b_2	29.2
b_3	31.6
b_4 (LSB)	37.0

Based on a 4-Bit DPT, we can observe that the amplifiers are not turned on at all instances. This is likely to lead to lower power consumption and hence a higher efficiency, compared to the case when a single amplifier is used and turned on at all instances. We believe that the power efficiency of this system is implementation dependent. An upper bound for the power efficiency is the duty cycle, which implies that the minimum power dissipated by these amplifiers is equal to the symbol rate multiplied by the switching time of the technology used. The estimated maximum efficiency is approximately equal to 1 - duty cycle = 1 - (switching time of transistor $\times$ data rate). Hence, for a 20 GHz technology, the estimated maximum efficiency for a data rate of 480 Mbps is in the neighbourhood of 95%.

C Gain variation, based on Monte Carlo simulation

In practice, the gain of each bit will deviate from the desired gain due to manufacturing variations. This was first reported in [6], where it is assumed there are no correlations between the amplifiers. In general, components within the same die follow a positive correlation, and hence the above assumption of zero correlation between the amplifiers represents the worst case.

In order to estimate the effects of gain mismatches among the

Table 3: Calculation of Probability Density Function from simulated CCDF result.

$\{b_1, b_2, b_3, b_4\}$	SignalRange_dB (dB)	Absolute power (dBm)	CCDF (%)	CDF (%)	PDF (%)
0000	$<$ -15.033	$<$ -39.578	100	0	37
0001	-15.033	-39.578	63	37	10
0010	-9.012	-33.557	53	47	6
0011	-5.490	-30.035	47	53	12
0100	-2.992	-27.537	35	65	8
0101	-1.053	-25.598	27	73	8
0110	0.530	-24.015	19	81	6.5
0111	1.869	-22.676	12.5	87.5	5
1000	3.029	-21.516	7.5	92.5	3.75
1001	4.052	-20.493	3.75	96.25	0.75
1010	4.967	-19.578	3	97	0.5
1011	5.795	-18.750	2.5	97.5	0.8
1100	6.551	-17.994	1.7	98.3	0.45
1101	7.246	-17.299	1.25	98.75	0.45
1110	7.890	-16.655	0.8	99.2	0.8
1111	8.489	-16.056	0	100	0

different parallel stages have on the EVM, a Monte Carlo (MC) analysis has been performed. The MC analysis is performed for a 4-bit DPT, at 480 Mbps, with the following steps:

1. An additional factor, k_i, is included for each amplifier in (4), as follows:

$$f_{mc,i}(x) = k_i \times \frac{1}{2^i} \times n \times y'. \quad (5)$$

2. An independent gaussian distribution has been assumed for each of $\{k_1, k_2, k_3, k_4\}$.

3. In order to model intra-die variations, the mean for each additional factor is set at 1, and the standard deviation is chosen to be 0.1 of the nominal value such that approximately 99% of the observations fall within $\pm 30\%$ of the mean value.

4. 100 runs have been performed, based on randomized values generated for $\{k_1, k_2, k_3, k_4\}$.

The result is plotted in Fig. 5. As we can observe, the EVM spreading is between -28 dB and -15 dB, where 85 runs meet the EVM requirement. Hence, this design is likely to be robust for a gain spread of up to $\pm 30\%$ between different amplifiers. This also suggests that the architecture should be feasible for the 90 nm technology and beyond.

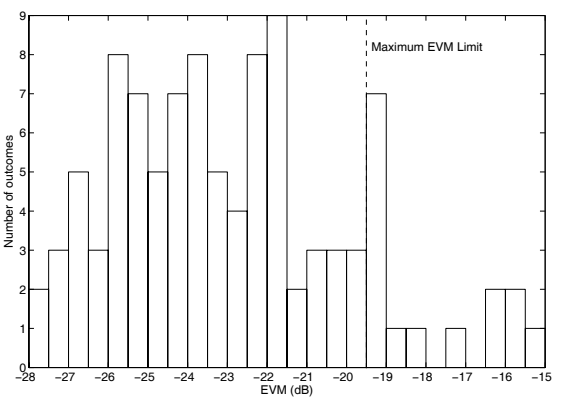

Figure 5: Histogram of EVM for gain variations in a 4-stage DPT.

IV Conclusion

A digital polar transmitter, based on an array of parallel amplifiers, has been proposed for UWB system, based on MBOA standards. A minimum of 4 parallel linear amplifiers is required for UWB signals using OFDM with QPSK modulation. Next, it is found that each amplifier is turned on for at most 37% for a burst of UWB signal. This parallel architecture is likely to result in a lower power consumption, and hence higher efficiency, compared to a single amplifier architecture. The maximum efficiency is likely to be dependent on the technology used. Maximum efficiency is estimated to be nearly 95% for a current technology for a data rate of 480 Mbps. Furthermore, the requirement for the individual device size can also be relaxed. Finally, a Monte Carlo analysis suggests that the architecture is likely to be robust for gain variation, due to manufacturing spread, of up to $\pm 30\%$ between different amplifiers.

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