ABSTRACT
The PhD project described in this paper aims to use word-length optimization techniques to automatically optimize the dynamic power consumption of high-level descriptions of DSP algorithms intended for implementation on FPGA, before or during synthesis. By developing models which can quickly estimate the power consumed by a system from a high-level description of the algorithm it implements, our work will allow for existing word-length optimization techniques to minimize the power consumption of a system, subject to acceptable signal distortion constraints.

1. INTRODUCTION
Power consumption in new FPGA devices is continuing to rise due to increasing logic density and clock rates in shrinking chip packages. High power consumption in FPGAs is becoming expensive as chips now require more expensive packaging and thermal dissipation solutions to prevent over-heating, whilst designs intended for use in battery-powered devices have even more stringent power consumption requirements due to restricted battery life and little opportunity for heat dissipation.

Reducing the power consumption of a system to meet a required constraint is a time consuming task for hardware designers. Faced with shortening design cycles and increasing design complexity, it is clear that hardware designers would greatly benefit from tools which can automatically optimize the power consumption of a system.

Our work focuses on using word-length optimization as a technique for reducing the power consumption in a system. Word-length optimization takes advantage of the fact that algorithms implemented entirely in hardware can be designed with datapaths containing precision customized processing units for each operation that must be computed by the algorithm. When compared to using a uniform signal scaling and precision for each operation in a datapath, designs that have been word-length optimized for area reduction have been seen to offer improvements in area usage of up to 80%, and as a side effect from this, power consumption has been reduced by up to 98% in extreme cases [1]. Figure 1 shows the power reductions achieved for adaptive filters of various orders, when using using word-length optimization for area as described in [1].

Word-length optimization is able to reduce the area in a system by assigning longer word-lengths to signals whose area-impact is low and whose noise-impact is high, and by assigning shorter word-lengths to those signals whose area impact is high and whose noise-impact is low. The aim is to minimize the implementation area whilst meeting user-specified constraints on the output SNR of the system. Note that the power consumption reductions achieved in Figure 1 are a side effect of word-length optimization for area. The

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Fig. 1. The power consumed by adaptive filters of various orders, when using: the minimum uniform word-length and uniform scaling for each signal to achieve a system output Signal to Noise Ratio of 34dB (shown by circles), the minimum uniform word-length and individually optimized scaling to achieve the same SNR (shown by stars), and the individually optimized word-length and scaling (shown by crosses). Note that area optimization, rather than power optimization, was performed. Taken from [1].
The aim of this PhD project is to use dynamic power consumption as the optimization goal for word-length optimization, rather than area, in order to get larger reductions in power.

Better results for power consumption reduction can be expected from word-length optimization for power (rather than for area) as some arithmetic components in a system may consume significantly more power consumption than others (and hence provide extra opportunity for word-length optimization). These differences will not only be due to area differences between components. The input signals to a component, whether a component is internally pipelined, and the capacitance of a component’s output connections are just some of the factors involved that can cause large differences in the power consumption between components.

The heuristic used in [1] to optimize the word-lengths in a system goes through many iterations in order to minimize area, where one signal’s word-length is reduced by one bit in each iteration. In each iteration the signal that provides the largest area pay-off, when its word-length is reduced as much as possible without violating error constraints, is found, and its word-length is then decreased by one bit.

This process obviously involves a very large number of iterations that make small changes to a design, estimate its resulting area, and then proceed according to this estimate. To optimize a system for power consumption this heuristic must be modified so that power consumption estimates, rather than area estimates, are performed. Estimating the dynamic power consumption of a system synthesized for FPGA is a much more computationally intensive process than estimating its area however. Power consumption estimates made using the low-level power estimation tool XPower, available from Xilinx, can take from several minutes to over a day to complete, for large systems. Synthesizing, mapping, placing and routing a design can also take a significant amount of time, and considering the number of iterations involved in the word-length optimization process, it is clear that power estimates obtained from low-level simulation using XPower, or even obtained through some simpler estimation technique from a low-level description of a system, would lead to excessively long computation times to find a solution to the word-length optimization problem.

2. FAST ESTIMATES OF POWER CONSUMPTION

Our work is currently focused on providing very fast estimates of the power consumption in a system, given only a high-level description (i.e., pre-synthesis) of the system’s structure. Power consumption macro-models have been identified as a suitable technique for estimating the power consumed in Look-Up Tables (LUTs) by arithmetic components. Work in [2] presented macro-models, parameterized by word-length, that can estimate the power consumed in adder and multiplier components, given word-level statistical information regarding the input signals to each component, assuming that these input signals are glitch-free, and have a mean value of zero. The signal statistics used are the variance of the signal and their lag-1 auto-correlation coefficient. This work was extended in [3] to allow for input signals with non-zero mean values, where it was also shown that there exists a direct link between the power consumed in LUTs by an arithmetic component and in the configurable routing wires that make internal connections between the LUTs of that component. Power estimates for a system can be calculated using these macro-models in a fraction of a second, whilst, as mentioned earlier, estimates from low-level simulation take from minutes to days for large systems. The power consumption estimates made by the work in [3] come at a slight cost in estimate accuracy, the mean relative error of which is at worst 7.2% compared to estimates from XPower.

In the short-term, our work aims to extend the power models in [2, 3] to estimate other power consuming effects which these models are unable to account for. Firstly, these models are being extended to handle arithmetic components whose inputs are not registered, i.e., inputs that may contain glitches. Preliminary investigations indicate that such components have significantly higher power consumption than input-registered components, and as such they are likely to provide further opportunities for word-length optimization for power to reduce power consumption over area optimal systems. Secondly, although the power consumed by the configurable routing wires within arithmetic components can be estimated using [3], there remains the problem of estimating the power consumed in routing wires between components, i.e., inter-component routing power. As the placement of components is not known at the pre-synthesis stage models will need to be developed to estimate the capacitance of these inter-component routing wires in order to allow the power consumed in them to then be estimated.

Our long-term goal is to integrate these power consumption estimation models into a word-length optimization tool, and to investigate the reductions in power consumption it offers. Other high-level power optimization techniques may also be considered in the future.

3. REFERENCES

