INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Monday, 28 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible

First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke
Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.
The Questions

1. a) Figure 1.1 (See the colour supplementary sheet) shows the layout of a CMOS cell with three inputs A, B and C, and two outputs OUT1 and OUT2. Extract and draw the transistor-level schematic diagram. [10]

b) What function does this circuit perform? [2]

c) Draw the vertical cross sections through the chip along the lines PP’ and QQ’. Label your diagram and indicate the different types and levels of doping (e.g. p+, n+ etc). [8]

2. a) Using your own group design project as a reference, describe the proper procedure for designing a full-custom integrated circuit. [4]

b) Draw a diagram showing the hierarchy of cells used in the chip that your group designed. Comment on the partitioning of your design in light of the cell hierarchy. [4]

c) Outline your own personal contributions and justify any design decisions made. If you and your group were to design the same chip again, what if anything would you have done differently? [8]

d) Explain and assess the strategy you adopted for verifying and testing your chip. [4]
3. a) Assume that you are a project leader in a company designing an ASIC for a new product for the telecommunication market. You are told that the expected demand can be as high as 1 million units in the first year. The complexity of the circuit that your team is designing is around 50,000 gates. You are required to decide which technology you should implement this ASIC, i.e. full custom, standard cell, gate array or FPGA. State what additional information you must acquire before you can make your decision. After stating clearly any additional assumptions that you have made, explain and justify your decision.

b) Figure 3.1 shows the transistor level schematic of a standard cell design. It is known that T6 is a minimum sized transistor and all other transistors are appropriately sized. Given that the timing diagram for the input signals CLK, A and B is as shown in Figure 3.2, draw the timing diagram for the signals at P, Q, R and OUT. Label your timing diagram with the following four possible signal states: driven low (DL), driven high (DH), charged low (CL), charged high (CH) and don’t know (XX).

c) Hence, or otherwise, explain the function of this cell.
4. a) Implement the following Boolean function as a single compound (or complex) CMOS static gate.

\[ y = (a \cdot b + c \cdot d) \cdot e \]  

[4]

b) Assuming that all the n-channel transistors have minimum width and length for the given technology, and that the mobility of an n-channel transistor is twice that of a p-channel transistor, size your circuit correctly so that the worst case rise and fall times are approximately equal. 

[3]

c) Use symbolic layout representation (for example, a stick diagram), design the layout of your circuit. 

[5]

d) Figure 4.1 shows a tristate bus driver with transistor sizes shown relative to unit size. By applying the Theory of Logic Effort, design an inverter chain to drive the enable input \( e \) of 128 such tristate bus drivers. You may assume that the first stage of your inverter chain may present an input capacitance of 6 unit-sized transistors. State any assumptions made. 

[8]
5. Figure 5.1 shows a synchronous bit-serial comparator cell where A and B inputs receive two 8-bit unsigned binary numbers with MSB first. The cell can be in one of three states representing S0, S1 and S2 as shown in Figure 5.2. A logic ‘1’ on the R input resets the internal state of the cell to S0. The cell produces H and L outputs after one clock cycle delay which are respectively the higher and lower value of the input sequence in bit-serial form.

Design a transistor level implementation of this bit-serial comparator cell using a single phase clocking method.

6. (a) Discuss the advantages and disadvantages of:
(i) Pass-transistor logic
(ii) Dynamic logic

(b) Figures 6.1 and 6.2 show two pass-transistor logic gates. Derive the truth tables for the two logic gates.

(c) Hence or otherwise, deduce the function of these circuits.
Figure 1.1 Layout of a full-custom cell for Question 1
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: PYKC/TJWC
Second Marker: TJWC/PYKC
Solution to Question 1

a) This question tests student’s ability to understand a full custom layout. This circuit is actually relatively hard to extract due to the large number of transistors. However, if student notice the symmetry in the circuit, it makes it a lot easier.

b) This is a combinatorial full adder giving ~SUM and ~CARRY.

c) This part of the question tests student’s ability to relate the layout to the physical layout on the chip.
[8 marks]
Solution to Question 2

Each student was involved in a group design project to design a full-custom integrated circuit during the course. Since they were learning while doing the project, a number of mistakes were made. The four parts of this question are intended to test how much each student learned through this experience.

a) The following are some of the points expected to be discussed:
   • Clarify specification of project right from the start, avoid changing spec during design
   • Adhere to top down design approach as much as possible. Model chip behaviourally to verify chip function
   • Careful floorplanning early on for the entire chip
   • For cell based designs, define cell boundary size and terminal location
   • Use autoplace & route tools if possible
   • Consider test right at the beginning of the design cycle. Design a good test vectore file, and use it for regressive verification and testing
   • Maximize regularity and minimize different types of cell designs
   • Pitch-match cells where possible
   • Hierarchical design, both simulation and layout. Avoid excess use of hierarchy

   I also expect more individual answers depending on student’s chip design. [4 marks]

b) This part depends on student’s chip. [4 marks]

c) This part of the question allows for recognition of individual understanding of, and contribution to, the project. In particular students are expected to learn from what they have done and suggest improvements to both the tools they used and the nature of project undertaken. [8 marks]

d) I expect students to have at least a high level model of the chip to generate test vectors. I also expect them to consider test coverage and possibly some of design for test such as scan registers or even built-in self tests. [4 marks]
Solution to Question 3

(a) Additional factors affecting decision:

<table>
<thead>
<tr>
<th>Factors</th>
<th>Cell based or Gate array</th>
<th>FPGA</th>
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<tbody>
<tr>
<td>Available design time</td>
<td>1 Year or more</td>
<td>Short</td>
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<tr>
<td>Experience of members in the team</td>
<td>Moderate to good</td>
<td>Weak to moderate</td>
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<tr>
<td>How fixed is the specification?</td>
<td>Completely</td>
<td>Not completely</td>
</tr>
<tr>
<td>How sure is the volume of 1 million parts?</td>
<td>Very</td>
<td>Reasonable</td>
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<tr>
<td>Available development budget</td>
<td>High</td>
<td>Limited</td>
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<tr>
<td>How high is performance required?</td>
<td>V. High</td>
<td>Up to 100MHz clock</td>
</tr>
<tr>
<td>Sensitivity to part cost</td>
<td>High</td>
<td>Moderate</td>
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I will not even contemplate full custom chip. 50,000 gates is not a large enough chip to justify a full custom design. Either a gate array or cell based (with full mask set) could be justified. FPGA would probably be too expensive and too power hungry.

[5 marks]

(b)

(c) This is a positive edge triggered NAND gate.

[3 marks]
Solution to Question 4

(a) The circuit could be:

(b) See relative transistor sizing in (a)

(c) Layout depends on student’s design. Full marks for topologically correct design with sensible layout. Deduce marks for poor layout of transistors that potentially takes lots of room.

(d) The theory of Logic Effort is developed by Ivan Sutherland and is taught to our students as ways of sizing transistors.

- Electrical Effort \( F = (\text{no of drivers}) \times (\text{input load to enable signal}) / \text{input capacitance} \)
  \[ F = 128 \times 12/6 = 256. \]
- Optimal no of stages \( N = \log_4 F = 4. \)
- Each stage increase in size by \( 4^{\text{th}} \) root of 256 = 4. Hence the design is:
Solution to Question 5

This question tests student ability to design a relatively complex transistor level circuit from specification. A possible solution using single phase clocking (only one clock signal):

This solution is taken from M. Afghahi, “A 512 16-b Bit-Serial Sorter Chip”, IEEE JSSC, Vol 26, No 10, Oct 1991. The P blocks are inserted to allow domino circuit where N and P blocks must alternate. Therefore the double P-block inverters is really an all pass circuit.

[20 marks]
Solution to Question 6

(a) (i)
Pass transistor logic relies on passing logic level as well as gate control.
Advantages: More efficient in transistor count (especially for XOR functions)
Lower power, can be faster
Disadvantages: Difficult to simulate with logic simulators
Charge sharing problems
Need complementary signals
No restoring logic, therefore pass either weak ‘1’ or weak ‘0’
No synthesis/sizing tools

(ii) Dynamic logic (as oppose to static logic).
Advantages: Generally smaller (only need n-tree or p-tree)
Can be very fast
Disadvantages: Needs to distribute clock – possible skew problem
Only work with part of a clock cycle, tighter timing constraints
Clock cannot stop

(b)

<table>
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<th>P</th>
<th>Q</th>
<th>R</th>
<th>Y</th>
<th>Z</th>
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(c) This is obviously a full adder circuit Y= SUM, Z= carry.

[3 marks]
[3 marks]
[3 marks]
[12 marks]
[2 marks]