Lecture 2

Basic MOS Theory, SPICE Simulation, CMOS Fabrication

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Based on slides/material by...

- P. Cheung http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/index.html
- J. Rabaey http://bwrc.eecs.berkeley.edu/Classes/IcBook/instructors.html
- D. Harris http://www.cmosvlsi.com/coursematerials.html
  Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Addison Wesley
Recommended Reading

- J. Rabaey et. al. “Digital Integrated Circuits: A Design Perspective”: Chapter 2 (2.1 – 2.3), Chapter 3 (3.3)

- Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”: Chapter 2, Chapter 3 (3.2), Chapter 5.
Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules
MOS Transistor

- Shown here is the cross-section of an n-channel enhancement transistor:
- Substrate is moderately doped with p-type material. Substrate in digital circuit is usually connected to $V_{Gnd}$ (ground).
- The source and drain regions are heavily doped with n-type material through diffusion. These are often referred to as the diffusion regions.
Conduction Characteristics of MOS Transistors (for fixed Vds)

- MOS transistors are majority-carrier devices.
- For n-channel transistors, the majority carriers are electrons conducted through a channel.
- A positive gate voltage (w.r.t. substrate) enhances the number of carriers in the channel, and increases conduction.
- **Threshold voltage** $V_{tn}$ denotes the gate-to-source voltage above which conduction occurs.
- For **enhancement** mode devices, $V_{tn}$ is positive; for **depletion** mode devices, $V_{tn}$ is negative.
- p-channel devices are similar to n-channel devices, except that all voltages and currents are in opposite polarity.
Cross-Section of CMOS Technology
MOS transistors - Types and Symbols

- NMOS Enhancement
- NMOS Depletion
- PMOS Enhancement
- NMOS with Bulk Contact
Threshold Voltage: Concept

- **DS**: Drain to Source
- **G**: Gate
- **V_{GS}**: Gate to Source Voltage
- **n-channel**: Type of channel in the MOSFET
- **n+**: Doped regions
- **p-substrate**: Type of substrate in the MOSFET
- **Depletion Region**: Region where the depletion charge is created

The diagram illustrates the basic components and connections of a MOSFET, including the gate (G) and the source (S) and drain (D) terminals, along with the n-channel and p-substrate regions.
MOS transistor (1)

- Between the diffusion regions is the gate area formed from a layer of polycrystalline silicon (known as **polysilicon**). This is separated from the substrate by a layer of **thin oxide** (made of silicon dioxide). Polysilicon is a reasonable conductor and forms the gate electrode.

- Underneath the thin oxide and between the n+ regions is the **channel**. The channel is conducting when a suitable electric field is applied to the gate.

- Due to geometric symmetry, there are no distinctions between the source and drain regions. However, we usually refer the terminal with more positive voltage the drain (for n-type) and less positive voltage the source.

- For a zero gate bias and a positive $V_{DS}$, no current flows between the drain and source because of the two **reverse biased diodes** shown in the diagram. The drain and source are therefore isolated from each other.

- Assuming that the substrate is always at the most negative supply voltage, these two diode should never become forward bias under normal operation.
MOS transistor (2)

- When a positive voltage is applied to the gate, an electric field is produced across the substrate which attracts electrons toward the gate. Eventually, the area under the gate changes from p-type to n-type, providing a conduction path between the source and drain.
- The gate-source voltage $V_{GS}$ when a channel starts to form under that gate is called the \textbf{threshold voltage $V_T$}.
- The surface underneath the gate under this condition is said to be \textbf{inverted}. The surface is known as the \textbf{inversion layer}.
- As larger bias is applied to the gate the inversion layer becomes thicker.
- An other p-n junction exists between the inversion layer and the substrate. This diode junction is \textbf{field induced}. Contrast this with the p-n junction between the source (or drain) and the substrate, which is created by a metallurgical process.
The Threshold Voltage

\[ V_{T0} = \phi_{mS} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

Workfunction Difference

\[ V_T = V_{T0} + \gamma(\sqrt{-2\phi_F + V_{SB}}) - \sqrt{-2\phi_F} \]

with

\[ V_{T0} = \phi_{mS} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

and

\[ \gamma = \sqrt{2q\varepsilon Si NA/C_{ox}} \]
Current-Voltage Relations

MOS transistor and its bias conditions
Current-Voltage Relations

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$
Transistor in Saturation

\[ V_{GS} > V_{GS} - V_T \]

\[ V_{DS} > V_{GS} - V_T \]
MOS transistor (3)

- As a voltage is applied between the source and drain, the inversion layer becomes thinner at the drain terminal due to interaction between $V_G$ and $V_D$.
- If $V_{DS} < V_{GS} - V_T$, then the drain current $I_D$ is a function of both $V_{GS}$ and $V_{DS}$. Furthermore, for a given $V_{DS}$, $I_D$ increases linearly with $(V_{GS} - V_T)$. The transistor is said to be operating in its linear or resistive region.
- If $V_{DS} > V_{GS} - V_T$, then $V_{GS} < V_T$ and no inversion layer can exist at the drain terminal. The channel is said to be 'pinched-off'. The transistor is operating in the saturation region, where the drain current is dependent on $V_{GS}$ and is almost independent of $V_{DS}$. 
I-V Relation

(a) $I_D$ as a function of $V_{DS}$

(b) $\sqrt{I_D}$ as a function of $V_{GS}$ (for $V_{DS} = 5V$).

NMOS Enhancement Transistor: $W = 100 \ \mu m$, $L = 20 \ \mu m$
A model for manual analysis

\[ V_{DS} > V_{GS} - V_T \]

\[ I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ V_{DS} < V_{GS} - V_T \]

\[ I_D = k'_n \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \]

with

\[ V_T = V_{T0} + \gamma (\sqrt{2 \phi_F + V_{SB}} - \sqrt{2 \phi_F}) \]
Dynamic Behavior of MOS Transistor

\[
\begin{align*}
G & \quad C_{GS} \quad C_{GB} \\
S & \quad C_{SB} \\
B & \quad C_{GD} \\
D & \quad C_{DB}
\end{align*}
\]
The Gate Capacitance

\[ C_{\text{gate}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} WL \]
Average Gate Capacitance

Different distributions of gate capacitance for varying operating conditions

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>$C_{gb}$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$C_{ox}WL_{eff}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Triode</td>
<td>0</td>
<td>$C_{ox}WL_{eff}/2$</td>
<td>$C_{ox}WL_{eff}/2$</td>
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<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{ox}WL_{eff}$</td>
<td>0</td>
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</tbody>
</table>

- Most important regions in digital design: saturation and cut-off
Issues concerning Sub-Micron MOS Transistors

- Threshold Variations
- Parasitic Resistances
- Velocity Saturation
- Mobility Degradation
Threshold Variations

Long-channel threshold

Threshold as a function of the length (for low $V_{DS}$)

Drain-induced barrier lowering (for low $L$)

Low $V_{DS}$ threshold

$V_T$
Parasitic Resistances
Velocity Saturation (1)

(a) Velocity saturation

\[ v_{sat} = 10^7 \]

Constant mobility (slope = \(\mu\))

\[ E_{sat} = 1.5 \quad E \ (V/\mu m) \]

(b) Mobility degradation

\[ \mu_n \]

\[ \mu_n0 \]

\[ 700 \quad 250 \]

\[ 0 \quad 100 \ (V/\mu m) \]
Velocity Saturation (2)

(a) $I_D$ as a function of $V_{DS}$

(b) $I_D$ as a function of $V_{GS}$ (for $V_{DS} = 5$ V).

Linear Dependence on $V_{GS}$
Sub-Threshold Conduction

\[ \ln(I_D) = \begin{cases} \text{Subthreshold exponential region} & \text{for } V_{GS} < V_T \\ \text{Linear region} & \text{for } V_{GS} \geq V_T \end{cases} \]
Latch-up problem (1)

- The p+ region of the p-transistor, the n-well and the p- substrate form a parasitic pnp transistor T1.
- The n- well, the p- substrate and the p+ source of the n-transistor forms another parasitic npn transistor T2.
- There exists two resistors Rw and Rs due to the resistive drop in the well area and the substrate area.
Latch-up problem (2)

- T1 and T2 form a thyristor circuit.
- If Rw and/or Rs are not 0, and for some reason (power-up, current spike etc), T1 or T2 are forced to conduct, Vdd will be shorted to Gnd through the small resistances and the transistors.
- Once the circuit is 'fired', both transistors will remain conducting due to the voltage drop across Rw and Rs. The only way to get out of this mode is to turn the power off.
- This condition is known as **latch-up**.
- To avoid latch-up, substrate-taps (tied to Gnd) and well-taps (tied to Vdd) are inserted as frequently as possible. This has the effect of shorting out Rw and Rs.
Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules
What is SPICE Circuit Simulator?

- **SPICE** is a widely-used circuit-level simulator, originally from Berkeley.
- SPICE uses numerical techniques to solve nodal analysis of circuit. It supports the following:
  - Textual input to specify circuit & simulation commands
  - Text or graphical output format for simulation results
- You can use SPICE to specify these circuit components:
  - Resistors, Capacitors, Inductors
  - Independent sources (V, I), Dependent sources (V, I)
  - Transmission lines
  - Active devices (diodes, BJTs, JFETS, MOSFETS)
- You can use SPICE to perform the following types circuit analysis:
  - non-linear d.c.
  - non-linear transient
  - linear a.c.
  - Noise & temperature
SPICE MODELS

Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

Level 4 (BSIM): Emperical - Simple and Popular
### MAIN MOS SPICE PARAMETERS

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
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<tr>
<td>SPICE Model Index</td>
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<td>Zero-Bias Threshold Voltage</td>
<td>Vt0</td>
<td>Vt0</td>
<td>V</td>
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<td>Process Transconductance</td>
<td>k'</td>
<td>KP</td>
<td>A/V2</td>
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<td>Body-Bias Parameter</td>
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<td>Oxide Thickness</td>
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<td>Lateral Diffusion</td>
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<td>Surface Inversion Potential</td>
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<td>PHI</td>
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<td>Substrate Doping</td>
<td>NA,ND</td>
<td>NSUB</td>
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<td>Surface State Density</td>
<td>Qss/q</td>
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<td>cm-3</td>
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<td>Total Channel Charge Coefficient</td>
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<td>Type of Gate Material</td>
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<td>Surface Mobility</td>
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<td>U0</td>
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<td>Maximum Drift Velocity</td>
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<td>VMAX</td>
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<td>UCRIT</td>
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<td>Transverse Field Exponent (mobility)</td>
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# SPICE Parameters for Parasitics

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<tr>
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<th>Units</th>
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<td>Source resistance</td>
<td>$R_S$</td>
<td>RS</td>
<td>$\Omega$</td>
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<td>Drain resistance</td>
<td>$R_D$</td>
<td>RD</td>
<td>$\Omega$</td>
<td>0</td>
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<tr>
<td>Sheet resistance (Source/Drain)</td>
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<td>RSH</td>
<td>$\Omega_o$</td>
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<td>MJ</td>
<td>-</td>
<td>0.5</td>
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<td>Zero Bias Side Wall Junction Cap</td>
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<td>CJSW</td>
<td>F/m</td>
<td>0</td>
</tr>
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<td>MJSW</td>
<td>-</td>
<td>0.3</td>
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<td>Gate-Bulk Overlap Capacitance</td>
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<td>PB</td>
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# SPICE Transistors Parameters

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<td>Drawn Length</td>
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<td>L</td>
<td>m</td>
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<td>Effective Width</td>
<td>W</td>
<td>W</td>
<td>m</td>
<td>-</td>
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<td>Source Area</td>
<td>AREA</td>
<td>AS</td>
<td>m2</td>
<td>0</td>
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<tr>
<td>Drain Area</td>
<td>AREA</td>
<td>AD</td>
<td>m2</td>
<td>0</td>
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<td>Source Perimeter</td>
<td>PERIM</td>
<td>PS</td>
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<td>0</td>
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<td>Drain Perimeter</td>
<td>PERIM</td>
<td>PD</td>
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<td>Squares of Source Diffusion</td>
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<td>NRS</td>
<td>-</td>
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<tr>
<td>Squares of Drain Diffusion</td>
<td></td>
<td>NRD</td>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>
Fitting level-1 model for manual analysis

Select $k'$ and $\lambda$ such that best matching is obtained @ $V_{gs} = V_{ds} = V_{DD}$
VDD decreases

• Save dynamic power
• Protect thin gate oxides and short channels
• No point in high value because of velocity sat.

Vt must decrease to maintain device performance

But this causes exponential increase in OFF leakage

Major future challenge

<table>
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<tr>
<td>Channel length (µm)</td>
<td>0.4</td>
<td>0.3</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.1</td>
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<td>Gate oxide (nm)</td>
<td>12</td>
<td>7</td>
<td>6</td>
<td>4.5</td>
<td>4</td>
<td>4</td>
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<tr>
<td>VDD (V)</td>
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<td>2.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
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<tr>
<td>VT (V)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
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<tr>
<td>NMOS I_{Dsat} (mA/µm) (@ V_{GS} = V_{DD})</td>
<td>0.35</td>
<td>0.27</td>
<td>0.31</td>
<td>0.21</td>
<td>0.29</td>
<td>0.33</td>
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<tr>
<td>PMOS I_{Dsat} (mA/µm) (@ V_{GS} = V_{DD})</td>
<td>0.16</td>
<td>0.11</td>
<td>0.14</td>
<td>0.09</td>
<td>0.13</td>
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Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
Well and Substrate Taps

- Substrate must be tied to GND and n-well to \( V_{DD} \)

- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode

- Use heavily doped well and substrate contacts / taps
Inverter Mask Set

- Transistors and wires are defined by masks
- Cross-section taken along dashed line

![Inverter Mask Set Diagram]

- GND
- VDD
- substrate tap
- nMOS transistor
- pMOS transistor
- well tap
**Detailed Mask Views**

- **Six masks**
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO₂ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO₂

p substrate
Oxidation

- Grow SiO$_2$ on top of Si wafer
  - 900 – 1200°C with H$_2$O or O$_2$ in oxidation furnace
Photoresist

◆ Spin on photoresist
  • Photoresist is a light-sensitive organic polymer
  • Softens where exposed to light
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO₂, only enter exposed Si
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
Polysilicon Patterning

- Use same lithography process to pattern polysilicon

Diagram:
- Polysilicon
- p substrate
- n well
- Thin gate oxide
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion
N-diffusion cont.

- Strip off oxide to complete patterning step
P-diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact.

![Diagram of P-diffusion process](image)
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed
Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires
Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules
Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size $f = \text{distance between source and drain}$
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3 \ \mu\text{m}$ in 0.6 $\mu\text{m}$ process
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
## CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
Intra Layer Design Rules

- Same Potential:
  - Well: 0 or 6
  - Active: 3
  - Select: 2

- Different Potential:
  - Polysilicon: 2
  - Contact or Via: 2
  - Metal1: 3
  - Metal2: 4
Transistor Layout
Via’s and Contacts
Select Layer
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A’
Summary

- MOS transistor: majority carrier device – building block of integrated circuits

- SPICE: popular circuit level simulator that applies nodal analysis of circuit

- CMOS transistors are fabricated on silicon wafer
  - Lithography process
  - Different materials are deposited or etched in each step

- Layout rules: contract between IC designer and process engineer
  - Guidelines for constructing process masks