Lecture 4

Sequential Circuits

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Based on slides/material by…

- P. Cheung http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/index.html
- J. Rabaey http://bwrc.eecs.berkeley.edu/Classes/IcBook/instructors.html
- D. Harris http://www.cmosvlsi.com/coursematerials.html
  Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Addison Wesley
Recommended Reading


- Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”: Chapter 1 (1.4.9), Chapter 7 (7.3.1 – 7.3.5)
Outline

- Bi – Stability / Meta – Stability
- Latches
- Flip – flops
- Schmitt Trigger
- Multivibrator circuits
- Counters and sequential machines
Combinational vs. Sequential Logic

(a) Combinational

Output = $f(In)$

(b) Sequential

Output = $f(In, \text{Previous In})$
Sequential Logic

2 storage mechanisms
• positive feedback
• charge-based
Positive Feedback: Bi-Stability

\[ V_{i1} = V_{i2} = V_{o1} = V_{o2} \]

Diagram showing the voltage relationships:

- \( V_{i1} \) and \( V_{i2} \) are inputs.
- \( V_{o1} \) and \( V_{o2} \) are outputs.
- The circuit exhibits bistable behavior with feedback loops.

Points A, B, and C on the voltage curves illustrate the state transitions of the system.
Meta-Stability

- Gain should be larger than 1 in the transition region
Outline

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D Latch

- When CLK = 1, latch is transparent
  - D flows through to Q like a buffer
- When CLK = 0, the latch is opaque
  - Q holds its old value independent of D
- *transparent latch* or *level-sensitive latch*
D Latch Design

- Multiplexer chooses D or old Q

![D Latch Diagram]
D Latch Operation

CLK = 1

CLK = 0

CLK

D

Q
Latch Design

- Pass Transistor Latch
- Pros
  - Tiny
  - Low clock load
- Cons
  - $V_t$ drop
  - nonrestoring
  - backdriving
  - output noise sensitivity
  - dynamic
  - diffusion input

Used in 1970’s
Latch Design

- Transmission gate
  - No $V_t$ drop
  - Requires inverted clock

\[
\begin{align*}
\text{D} & \quad \text{Q} \\
\phi & \quad \phi
\end{align*}
\]
Latch Design

- Inverting buffer
  + Restoring
  + No backdriving
  + Fixes either
    - Output noise sensitivity
    - Or diffusion input
  - Inverted output
Latch Design

- Tristate feedback
  - Static
  - Backdriving risk

- Static latches are now essential
Latch Design

- Buffered input
  - Fixes diffusion input
  - Noninverting
Latch Design

- Buffered output
  - No backdriving

- Widely used in standard cells
  - Very robust (most important)
  - Rather large
  - Rather slow
  - High clock loading
Latch Design

- Datapath latch
  - Smaller, faster
  - Unbuffered input
Outline

- Bi – Stability / Meta – Stability
- Latches
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D Flip-flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- *positive edge-triggered flip-flop, master-slave flip-flop*
D Flip-flop Design

- Built from master and slave D latches
D Flip-flop Operation

CLK = 0

CLK = 1

CLK
Flip-Flop: Timing Definitions

- $t_{setup}$
- $t_{hold}$
- $t_{pFF}$

Data Stable regions:
- In
- Out

Flip-Flop: Timing Definitions

- $\phi$
- $t$

Sequential Circuits
Introduction to Digital Integrated Circuit Design
Lecture 4 - 24
Maximum Clock Frequency

\[ t_{p,\text{setup}} + t_{p,\text{comb}} + t_{\text{FF}} < T \]
Flip-Flop Design

- Flip-flop is built as pair of back-to-back latches.
Enable

- Enable: ignore clock when $en = 0$
  - Mux: increase latch D-Q delay
  - Clock Gating: increase $en$ setup time, skew
Reset

- Force output low when reset asserted
- Synchronous vs. asynchronous
Set / Reset

- Set forces output high when enabled
- Flip-flop with asynchronous set and reset
SR-Flip Flop

<table>
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<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>\overline{Q}</th>
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<td>Q</td>
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</table>
JK- Flip Flop

(a) Circuit diagram of a JK Flip Flop

(b) Truth table for a JK Flip Flop

\[
\begin{array}{ccc}
J_n & K_n & Q_{n+1} \\
0 & 0 & Q_n \\
0 & 1 & 0 \\
1 & 0 & 1 \\
1 & 1 & \overline{Q}_n \\
\end{array}
\]
Other Flip-Flops

- **Toggle Flip-Flop**

- **Delay Flip-Flop**
Master-Slave Flip-Flop

![Master-Slave Flip-Flop Diagram]
Edge Triggered Flip-Flop
Race Condition

- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*

![Diagram of race condition](image-url)
Nonoverlapping Clocks

- Nonoverlapping clocks can prevent races
  - As long as nonoverlap exceeds clock skew
- Can be used for safe design
  - Industry manages skew more carefully instead
CMOS Clocked SR-FlipFlop
Flip-Flop: Transistor Sizing
6 Transistor CMOS SR-Flip Flop
Charge-Based Storage

(a) Schematic diagram

(b) Non-overlapping clocks

Pseudo-static Latch
Master-Slave Flip-Flop

Overlapping Clocks Can Cause
- Race Conditions
- Undefined Signals
2 phase non-overlapping clocks
2-phase dynamic flip-flop
Flip-flop insensitive to clock overlap

C$^2$MOS LATCH
C²MOS avoids Race Conditions

(a) (1-1) overlap

(b) (0-0) overlap
**Pipelining**

![Diagram showing non-pipelined and pipelined versions of a digital integrated circuit design.](image)

<table>
<thead>
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<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
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<td>1</td>
<td>$a_1 + b_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$a_2 + b_2$</td>
<td>$</td>
<td>a_1 + b_1</td>
</tr>
<tr>
<td>3</td>
<td>$a_3 + b_3$</td>
<td>$</td>
<td>a_2 + b_2</td>
</tr>
<tr>
<td>4</td>
<td>$a_4 + b_4$</td>
<td>$</td>
<td>a_3 + b_3</td>
</tr>
<tr>
<td>5</td>
<td>$a_5 + b_5$</td>
<td>$</td>
<td>a_4 + b_4</td>
</tr>
</tbody>
</table>
Pipelined Logic using C²MOS

What are the constraints on $F$ and $G$?

NORA CMOS
NORA CMOS Modules

(a) \( \phi \)-module

(b) \( \bar{\phi} \)-module

Combinational logic

Latch
Doubled $\text{C}^2\text{MOS}$ Latches

Doubled n-$\text{C}^2\text{MOS}$ latch
TSPC - True Single Phase Clock Logic

Including logic into the latch

Inserting logic between latches
Master-Slave Flip-flops

(a) Positive edge-triggered $D$ flip-flop

(b) Negative edge-triggered $D$ flip-flop

(c) Positive edge-triggered $D$ flip-flop using split-output latches
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Schmitt Trigger

- VTC with hysteresis
- Restores signal slopes
Noise Suppression using Schmitt Trigger

- $V_{in}$
- $V_{M+}$
- $V_{M-}$
- $t_0$
- $t$
- $V_{out}$
- $t_0 + t_p$
- $t$
CMOS Schmitt Trigger

\[ V_{DD} \]

\[ V_{in} \]

\[ X \]

\[ V_{out} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]
Schmitt Trigger Simulated VTC
CMOS Schmitt Trigger (2)
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Multivibrator Circuits

- **Bistable Multivibrator**: flip-flop, Schmitt Trigger
- **Monostable Multivibrator**: one-shot
- **Astable Multivibrator**: oscillator
Transition-Triggered Monostable
Monostable Trigger (RC-based)

(a) Trigger circuit.

(b) Waveforms.
Astable Multivibrators (Oscillators)

Ring Oscillator

simulated response of 5-stage oscillator
Voltage Controller Oscillator (VCO)

- Current starved inverter
- Schmitt Trigger restores signal slopes

Graph showing propagation delay as a function of control voltage
Relaxation Oscillator

\[ T = 2 \left( \log_3 \right) RC \]
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One-bit counter implementation
One-bit counter operation

- All operations are performed as $s_{\phi_2}$.
- XOR computes next value of this bit of counter.
- NAND/inverter compute carry-out.
n-bit counter structure
Sequential machines

- Use memory elements to make primary output values depend on state + primary inputs.
- Varieties:
  - Mealy—outputs function of present state, inputs;
  - Moore—outputs depend only on state.
Sequential machine definition

- Machine computes next state $N$, primary outputs $O$ from current state $S$, primary inputs $I$.
- Next-state function:
  - $N = \delta(I,S)$.
- Output function (Mealy):
  - $O = \lambda(I,S)$. 
FSM structure
Summary

◆ Bi-stable sequential circuits
  • Latches (level sensitive circuits)
  • Flip – flops (edge triggered circuits)

◆ Non bi-stable sequential circuits
  • Schmitt Trigger (responds fast to a slowly changing input)
  • Multivibrator circuits
    ➤ Monostable (only one stable state – generates pulse of predetermined width)
    ➤ Astable (no stable states – output oscillates between two quasi stable states)