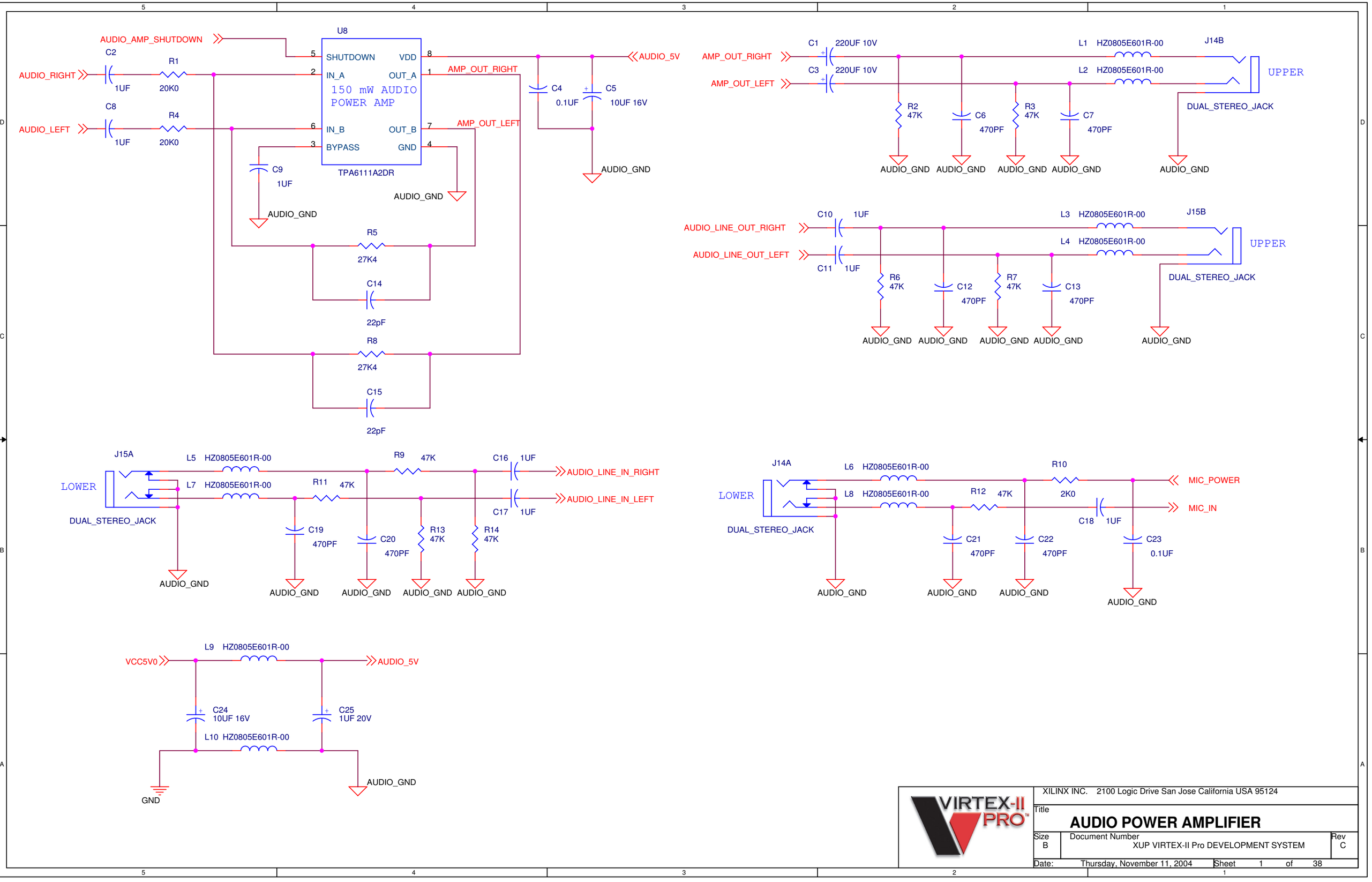

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title

AUDIO POWER AMPLIFIER

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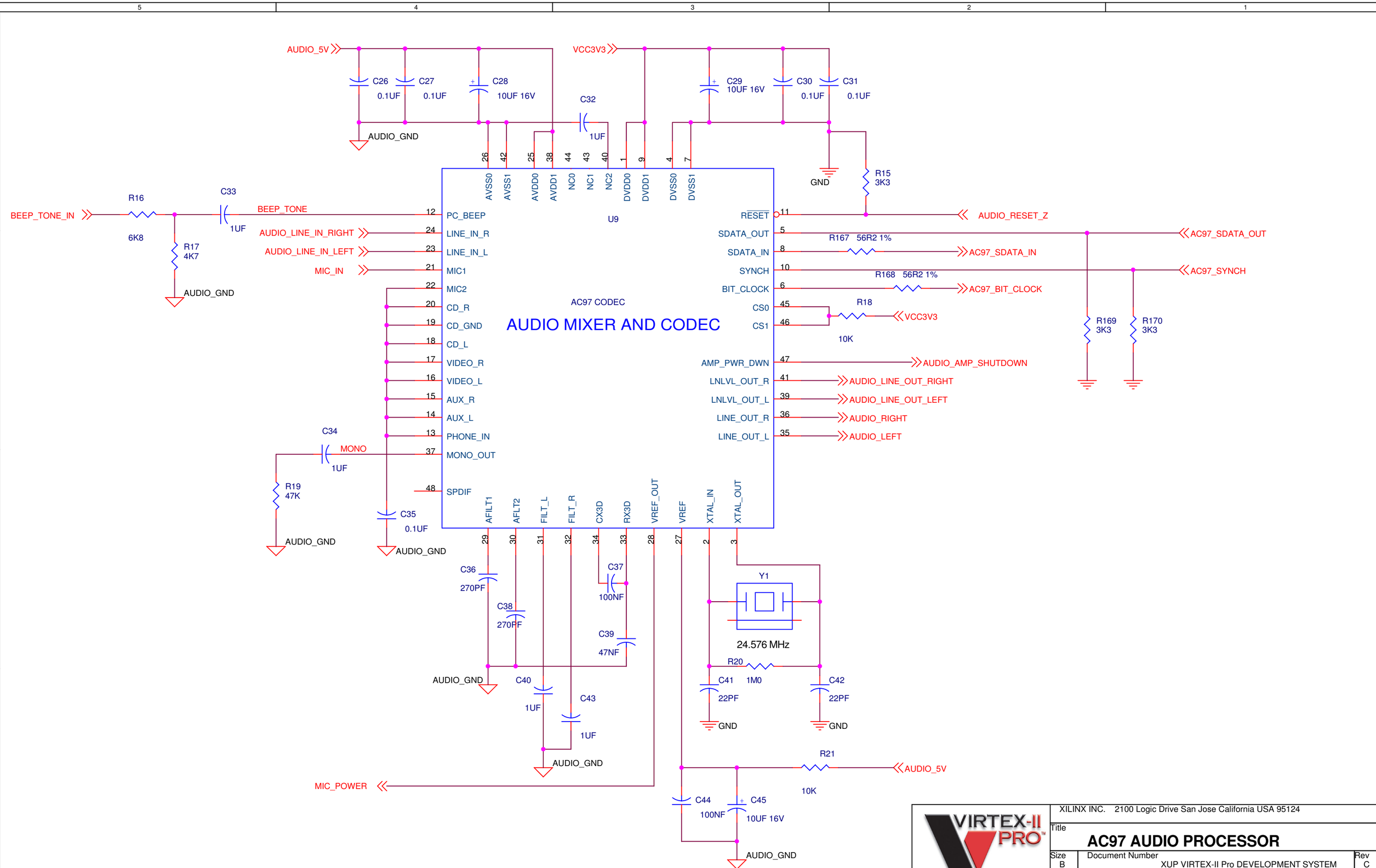

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **AC97 AUDIO PROCESSOR**

Size: B | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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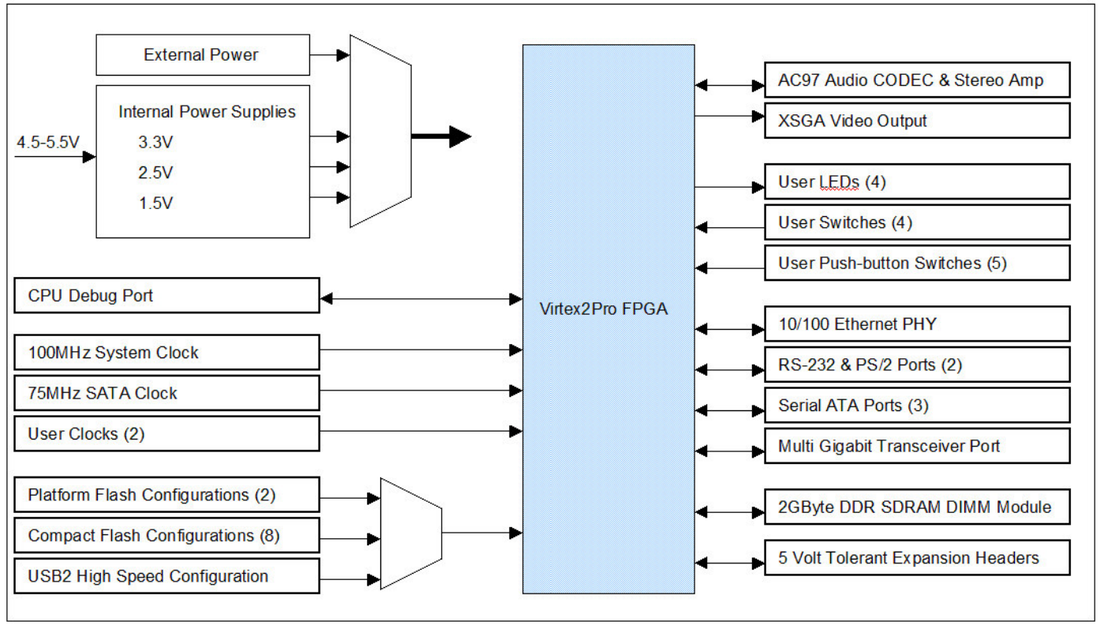

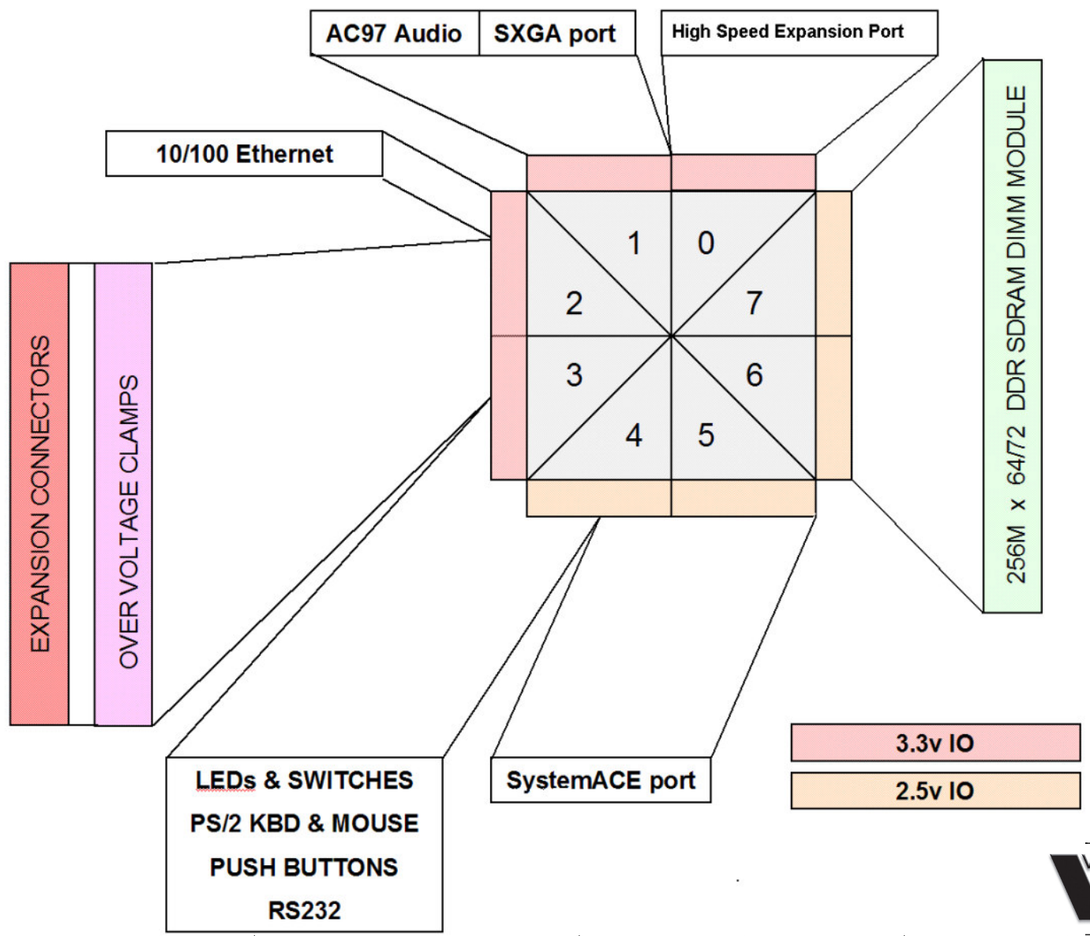

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Title: **BLOCK DIAGRAM & BANK CONNECTIONS**

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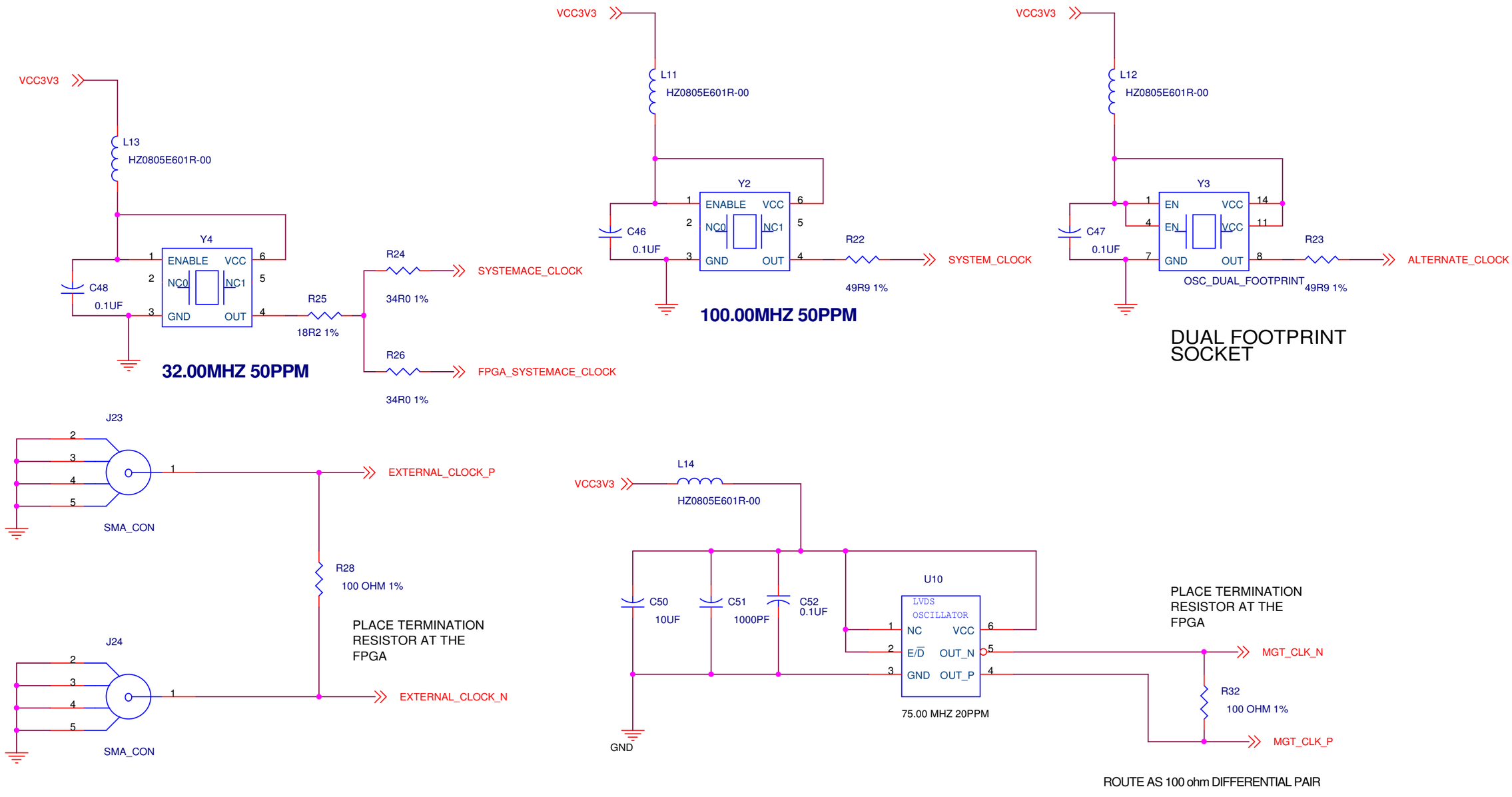

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Title: **CLOCKS**

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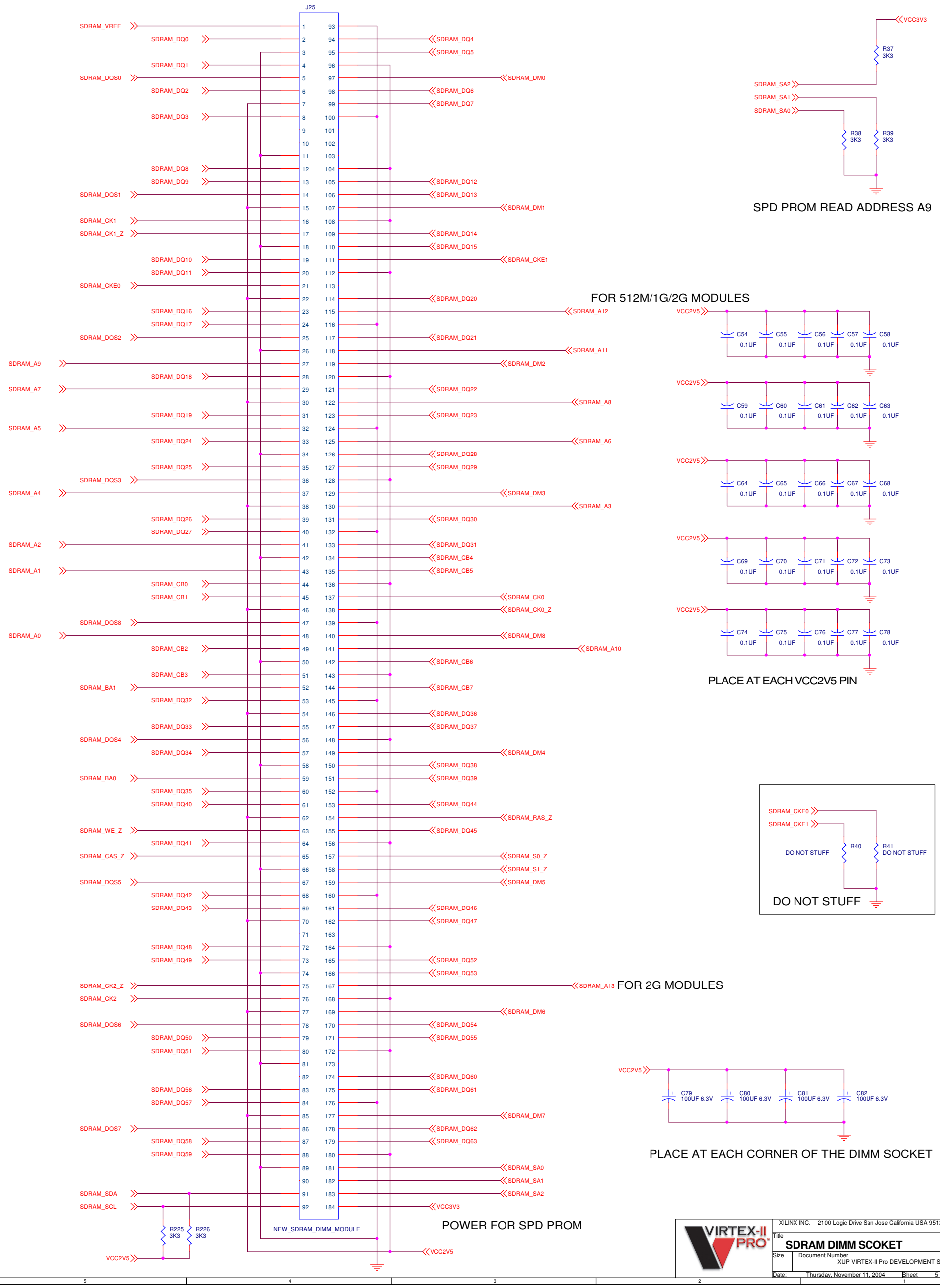

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **SDRAM DIMM SCOKET**

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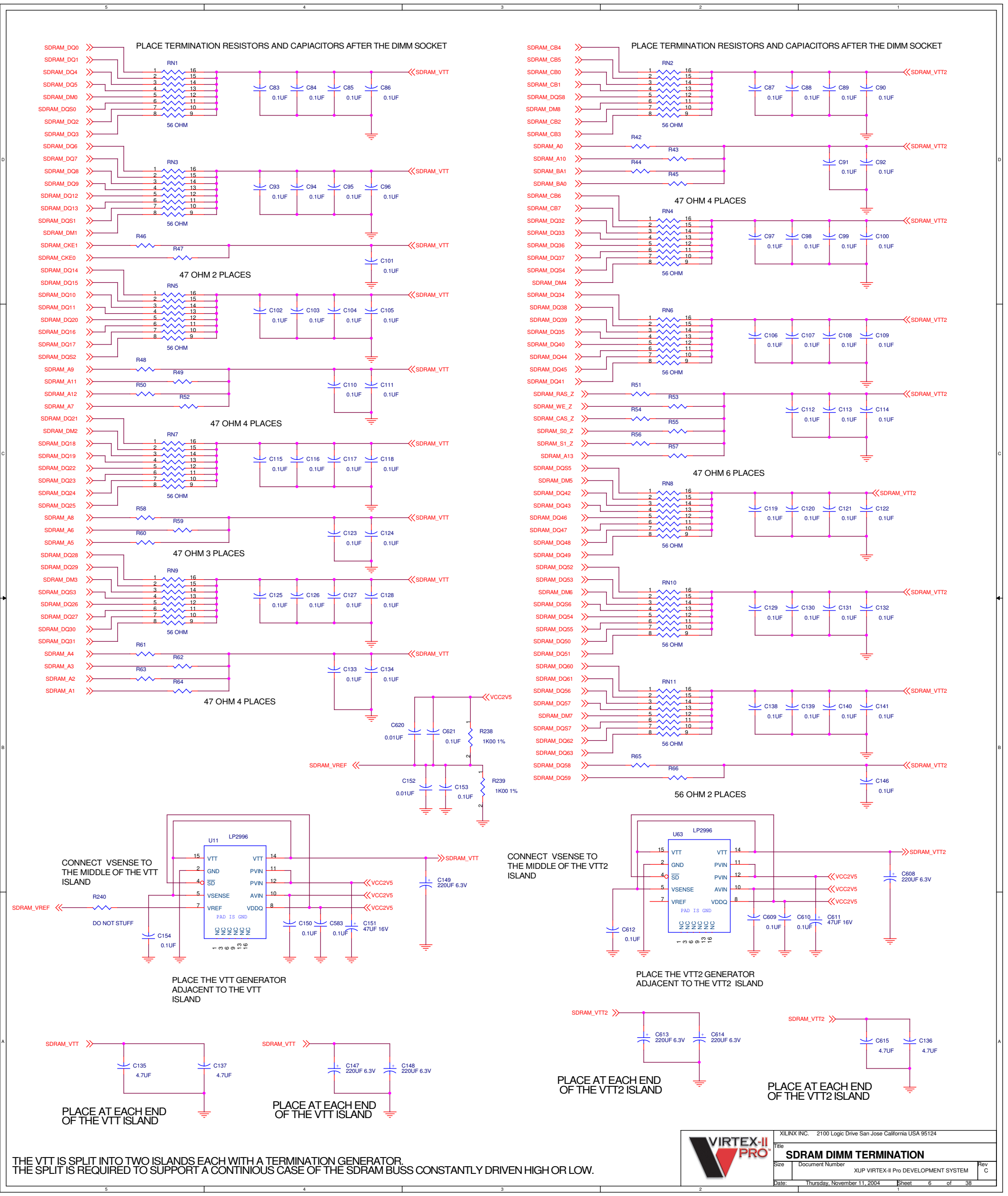
PLACE TERMINATION RESISTORS AND CAPIACITORS AFTER THE DIMM SOCKET
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
56 OHM
47 OHM 2 PLACES
47 OHM 4 PLACES
47 OHM 3 PLACES
47 OHM 6 PLACES
56 OHM 2 PLACES
SDRAM_VTT
SDRAM_VTT2
SDRAM_VREF
VCC2V5
U11
LP2996
U63
CONNECT VSENSE TO THE MIDDLE OF THE VTT ISLAND
CONNECT VSENSE TO THE MIDDLE OF THE VTT2 ISLAND
DO NOT STUFF
PAD IS GND
PLACE THE VTT GENERATOR ADJACENT TO THE VTT ISLAND
PLACE THE VTT2 GENERATOR ADJACENT TO THE VTT2 ISLAND
PLACE AT EACH END OF THE VTT ISLAND
PLACE AT EACH END OF THE VTT2 ISLAND
THE VTT IS SPLIT INTO TWO ISLANDS EACH WITH A TERMINATION GENERATOR.
THE SPLIT IS REQUIRED TO SUPPORT A CONTINIOUS CASE OF THE SDRAM BUSS CONSTANTLY DRIVEN HIGH OR LOW.
XILINX INC. 2100 Logic Drive San Jose California USA 95124
SDRAM DIMM TERMINATION
XUP VIRTEX-II Pro DEVELOPMENT SYSTEM
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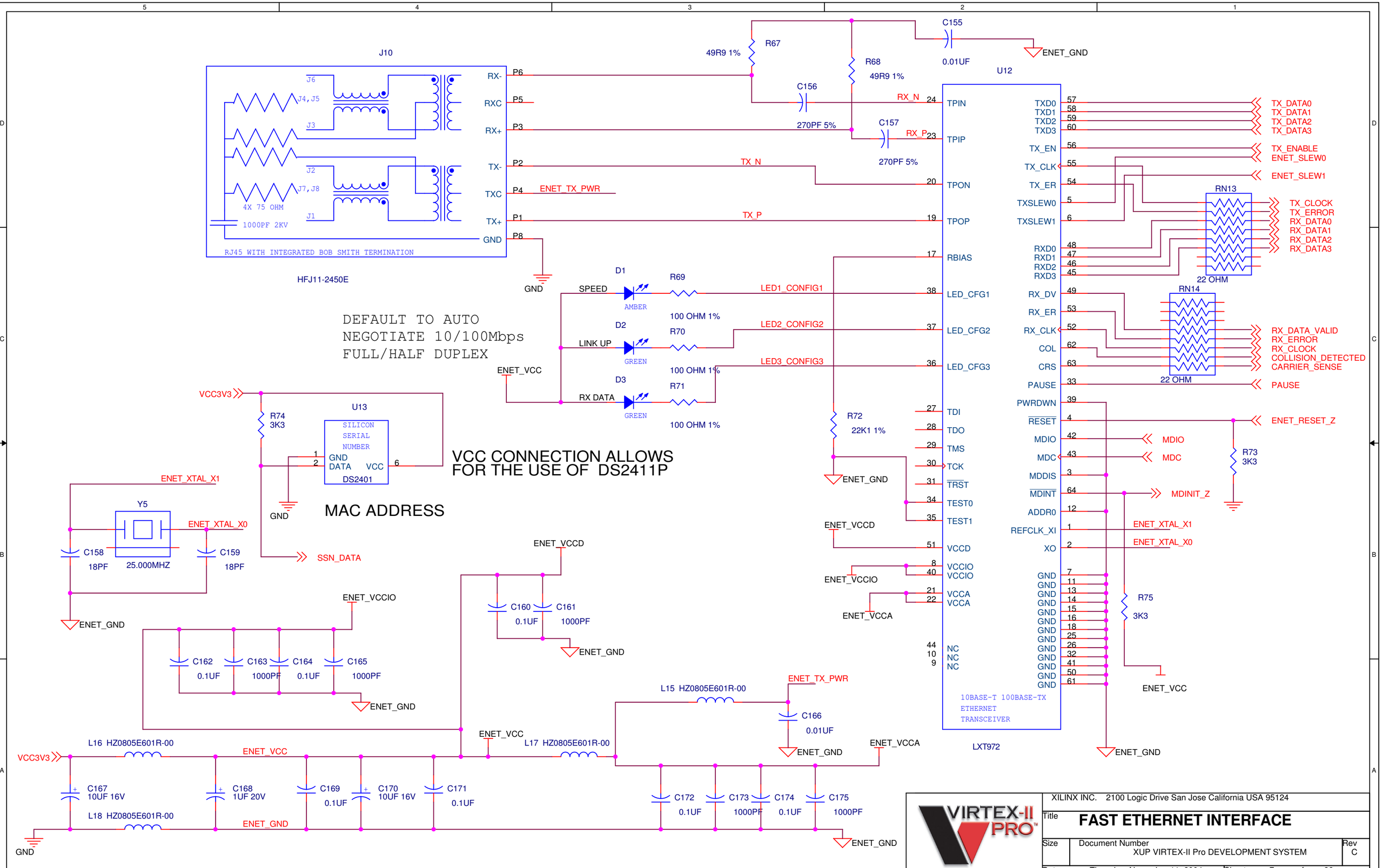
J10
RX-
RXC
RX+
TX-
TXC
TX+
GND
P6
P5
P3
P2
P4
P1
P8
J6
J4,J5
J3
J2
J7,J8
J1
4X 75 OHM
1000PF 2KV
RJ45 WITH INTEGRATED BOB SMITH TERMINATION
HFJ11-2450E
ENET_TX_PWR
GND
R67
49R9 1%
R68
49R9 1%
C155
0.01UF
ENET_GND
C156
270PF 5%
C157
270PF 5%
RX_N
RX_P
TX_N
TX_P
U12
TPIN
TPIP
TPON
TPOP
RBIAS
LED_CFG1
LED_CFG2
LED_CFG3
TDI
TDO
TMS
TCK
TRST
TEST0
TEST1
VCCD
VCCIO
VCCA
NC
TXD0
TXD1
TXD2
TXD3
TX_EN
TX_CLK
TX_ER
TXSLEW0
TXSLEW1
RXD0
RXD1
RXD2
RXD3
RX_DV
RX_ER
RX_CLK
COL
CRS
PAUSE
PWRDWN
RESET
MDIO
MDC
MDDIS
MDINT
ADDR0
REFCLK_XI
XO
GND
10BASE-T 100BASE-TX
ETHERNET
TRANSCEIVER
LXT972
TX_DATA0
TX_DATA1
TX_DATA2
TX_DATA3
TX_ENABLE
ENET_SLEW0
ENET_SLEW1
RN13
22 OHM
TX_CLOCK
TX_ERROR
RX_DATA0
RX_DATA1
RX_DATA2
RX_DATA3
RN14
22 OHM
RX_DATA_VALID
RX_ERROR
RX_CLOCK
COLLISION_DETECTED
CARRIER_SENSE
PAUSE
ENET_RESET_Z
R73
3K3
MDIO
MDC
MDINIT_Z
ENET_XTAL_X1
ENET_XTAL_X0
R75
3K3
ENET_VCC
ENET_GND
D1
SPEED
AMBER
R69
100 OHM 1%
D2
LINK UP
GREEN
R70
100 OHM 1%
D3
RX DATA
GREEN
R71
100 OHM 1%
LED1_CONFIG1
LED2_CONFIG2
LED3_CONFIG3
R72
22K1 1%
ENET_VCC
DEFAULT TO AUTO
NEGOTIATE 10/100Mbps
FULL/HALF DUPLEX
VCC3V3
R74
3K3
U13
SILICON
SERIAL
NUMBER
GND
DATA
VCC
DS2401
VCC CONNECTION ALLOWS
FOR THE USE OF DS2411P
MAC ADDRESS
SSN_DATA
ENET_XTAL_X1
Y5
ENET_XTAL_X0
C158
18PF
25.000MHZ
C159
18PF
ENET_VCCD
ENET_VCCIO
ENET_VCCA
C160
0.1UF
C161
1000PF
C162
0.1UF
C163
1000PF
C164
0.1UF
C165
1000PF
L15 HZ0805E601R-00
ENET_TX_PWR
C166
0.01UF
L16 HZ0805E601R-00
L17 HZ0805E601R-00
L18 HZ0805E601R-00
C167
10UF 16V
C168
1UF 20V
C169
0.1UF
C170
10UF 16V
C171
0.1UF
C172
0.1UF
C173
1000PF
C174
0.1UF
C175
1000PF
VIRTEX-II PRO
XILINX INC. 2100 Logic Drive San Jose California USA 95124
Title
FAST ETHERNET INTERFACE
Size
Document Number
XUP VIRTEX-II Pro DEVELOPMENT SYSTEM
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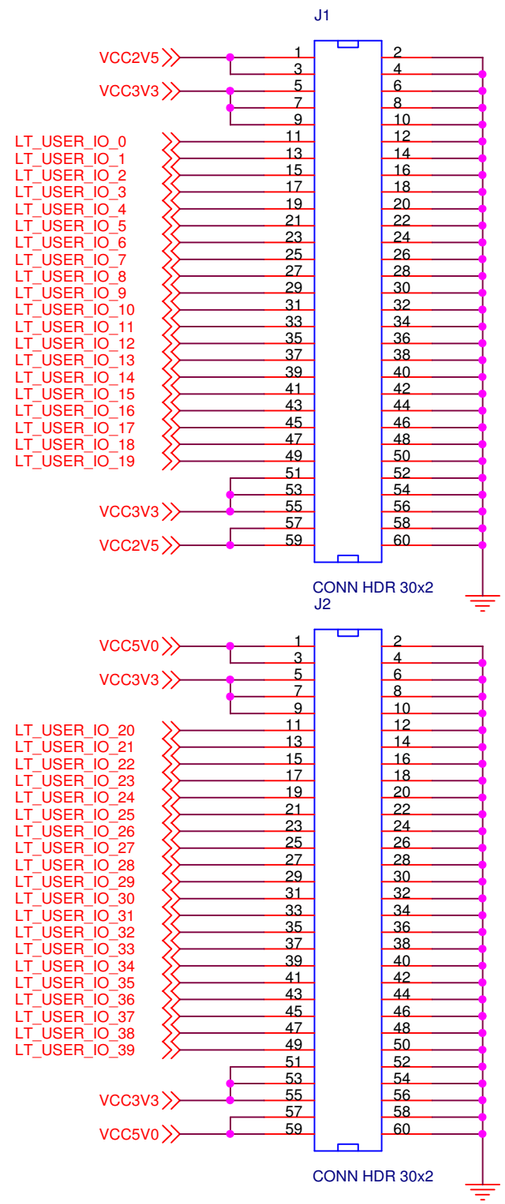
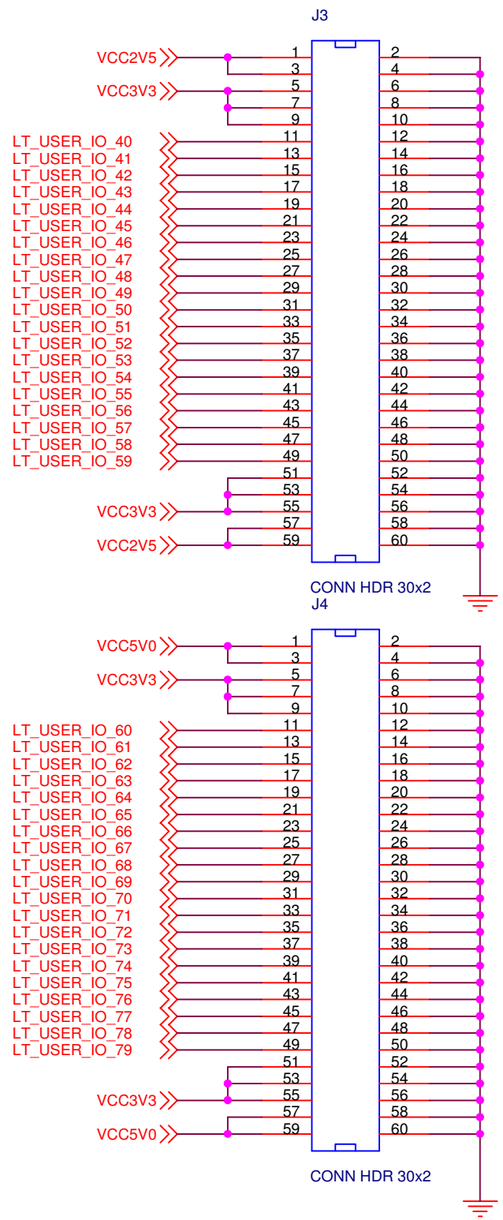
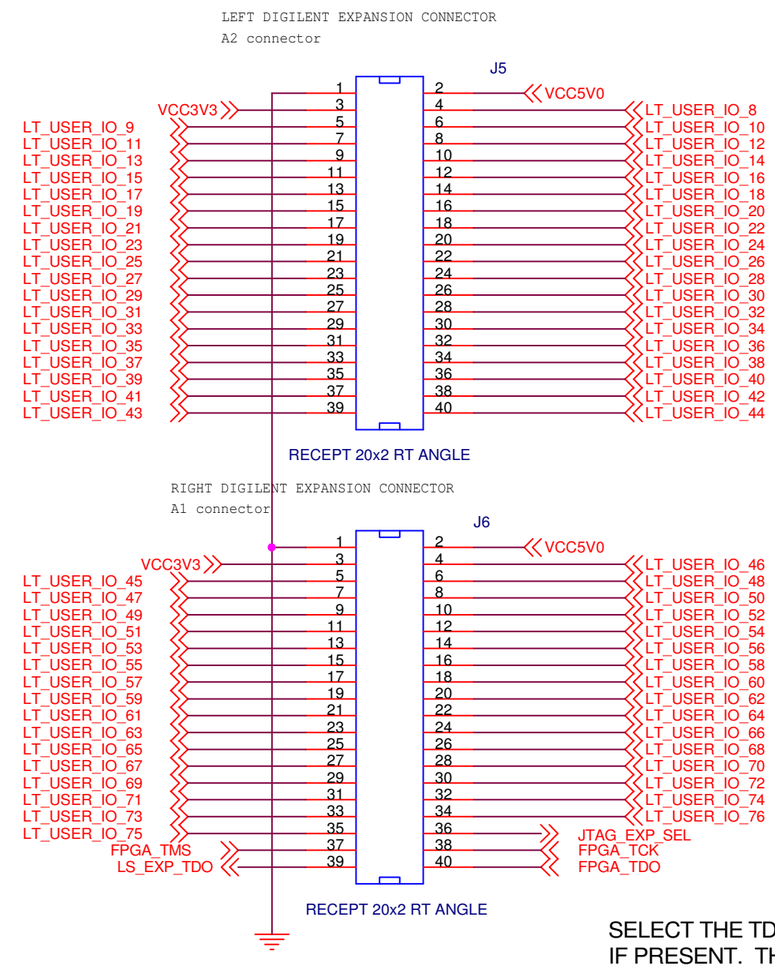
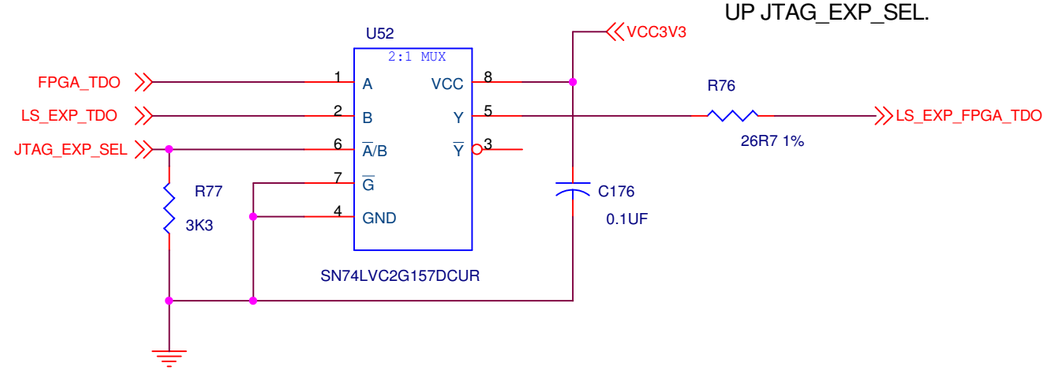






SELECT THE TDO FROM THE EXPANSION BOARD IF PRESENT. THE EXPANSION BOARD WILL PULL UP JTAG_EXP_SEL.



The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

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Title: **EXPANSION PORTS**

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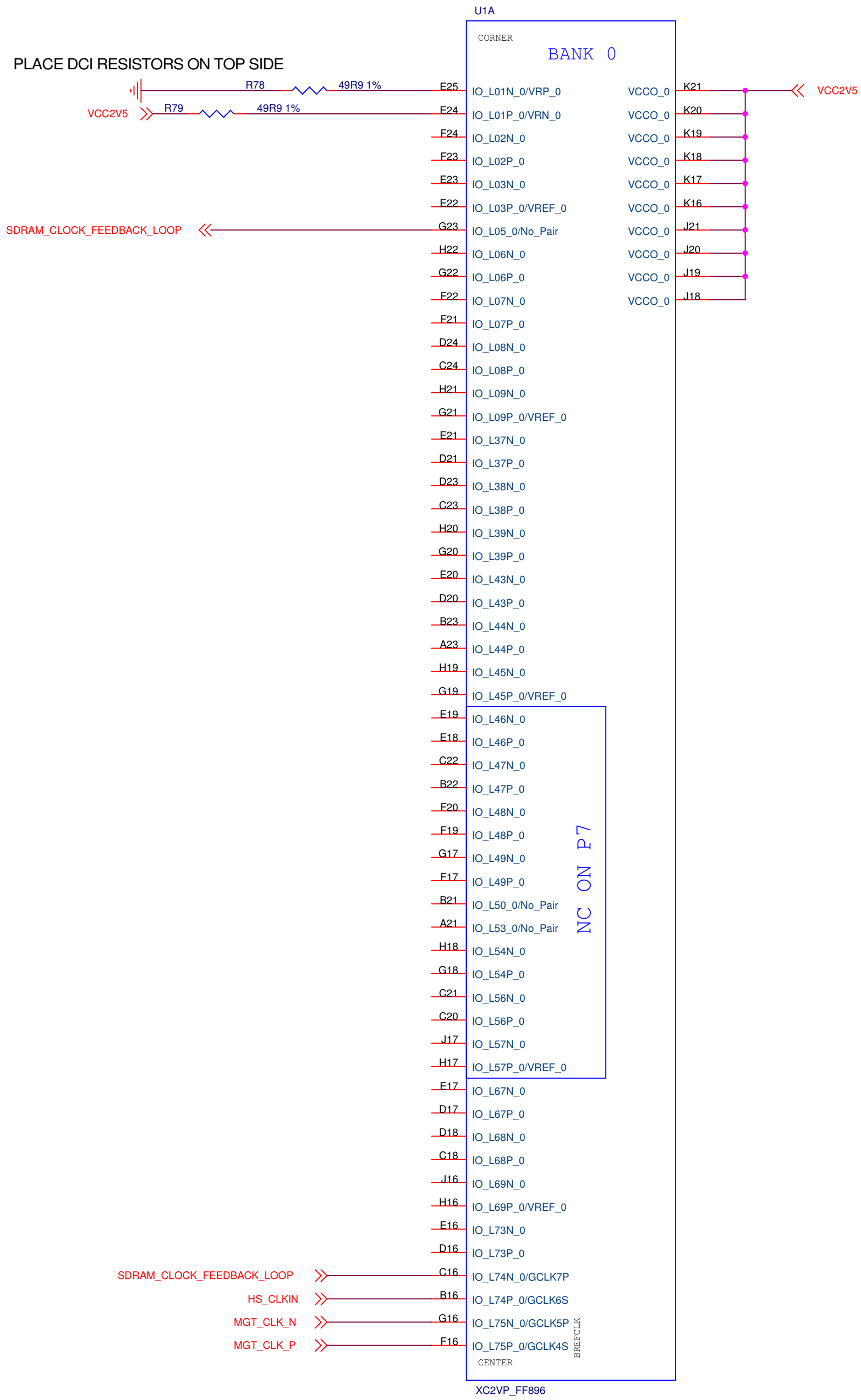

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Title
BANK0 IOS

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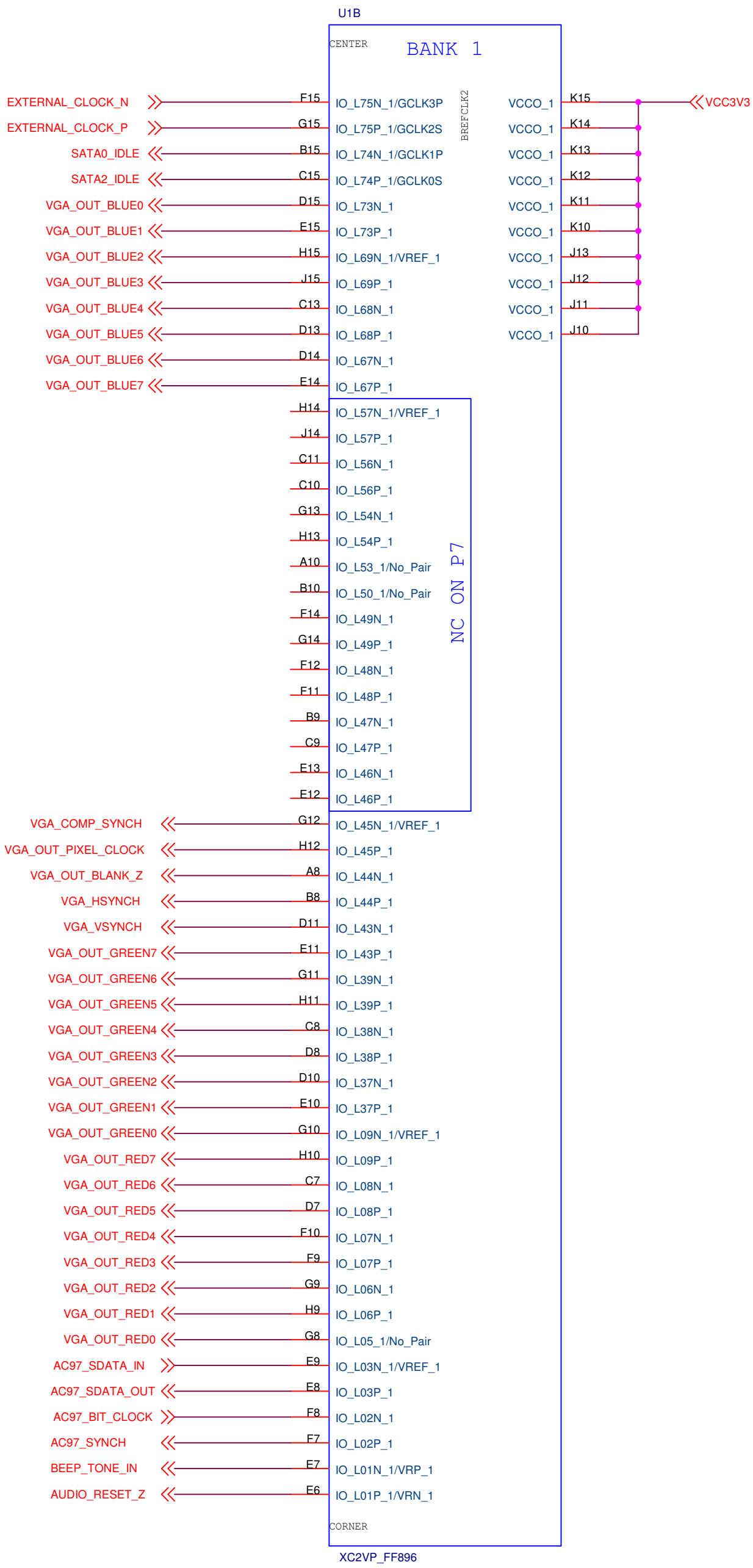

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Title
BANK1 IOS

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U1C

CORNER BANK 2

ENET_SLEW1	A3	IO_L01N_2/VRP_2	VCCO_2	R10	VCC3V3
ENET_SLEW0	B3	IO_L01P_2/VRN_2	VCCO_2	P10	
ENET_RESET_Z	G6	IO_L02N_2	VCCO_2	N10	
MDINIT_Z	G5	IO_L02P_2	VCCO_2	N9	
CARRIER_SENSE	C5	IO_L03N_2	VCCO_2	M10	
COLLISION_DETECTED	D5	IO_L03P_2	VCCO_2	M9	
TX_DATA3	C2	IO_L04N_2/VREF_2	VCCO_2	L10	
TX_DATA2	C1	IO_L04P_2	VCCO_2	L9	
TX_DATA1	J8	IO_L05N_2	VCCO_2	K9	
TX_DATA0	J7	IO_L05P_2	VCCO_2	J9	
TX_ENABLE	C4	IO_L06N_2			
TX_CLOCK	D3	IO_L06P_2			
	D2	IO_L31N_2			
	D1	IO_L31P_2			
	H6	IO_L32N_2			
	H5	IO_L32P_2			
HS_CLKOUT	E4	IO_L33N_2			
HS_CLKIO	E3	IO_L33P_2			
HS_USER_IO_40	E2	IO_L34N_2/VREF_2			
HS_USER_IO_39	E1	IO_L34P_2			
HS_USER_IO_38	K8	IO_L35N_2			
HS_USER_IO_37	K7	IO_L35P_2			
HS_USER_IO_36	F4	IO_L36N_2			
HS_USER_IO_35	F3	IO_L36P_2			
HS_USER_IO_34	F2	IO_L37N_2			
HS_USER_IO_33	F1	IO_L37P_2			
HS_USER_IO_32	J6	IO_L38N_2			
HS_USER_IO_31	J5	IO_L38P_2			
HS_USER_IO_30	G4	IO_L39N_2			
HS_USER_IO_29	G3	IO_L39P_2			
HS_USER_IO_28	G2	IO_L40N_2/VREF_2			
HS_USER_IO_27	G1	IO_L40P_2			
HS_USER_IO_26	L8	IO_L41N_2			
HS_USER_IO_25	L7	IO_L41P_2			
	H4	IO_L42N_2			
	H3	IO_L42P_2			
TX_ERROR	H2	IO_L43N_2			
RX_ERROR	J2	IO_L43P_2			
RX_CLOCK	M8	IO_L44N_2			
RX_DATA_VALID	M7	IO_L44P_2			
RX_DATA0	K6	IO_L45N_2			
RX_DATA1	K5	IO_L45P_2			
RX_DATA2	J1	IO_L46N_2/VREF_2			
RX_DATA3	K1	IO_L46P_2			
MDC	M6	IO_L47N_2			
MDIO	M5	IO_L47P_2			
PAUSE	J4	IO_L48N_2			
SSN_DATA	J3	IO_L48P_2			
EXP_IO_0	K2	IO_L49N_2			
EXP_IO_1	L2	IO_L49P_2			
EXP_IO_2	N8	IO_L50N_2			
EXP_IO_3	N7	IO_L50P_2			
EXP_IO_4	K4	IO_L51N_2			
EXP_IO_5	K3	IO_L51P_2			
EXP_IO_6	L1	IO_L52N_2/VREF_2			
EXP_IO_7	M1	IO_L52P_2			
EXP_IO_8	N6	IO_L53N_2			
EXP_IO_9	N5	IO_L53P_2			
EXP_IO_10	L5	IO_L54N_2			
EXP_IO_11	L4	IO_L54P_2			
EXP_IO_12	M2	IO_L55N_2			
EXP_IO_13	N2	IO_L55P_2			
EXP_IO_14	P9	IO_L56N_2			
EXP_IO_15	R9	IO_L56P_2			
EXP_IO_16	M4	IO_L57N_2			
EXP_IO_17	M3	IO_L57P_2			
EXP_IO_18	N1	IO_L58N_2/VREF_2			
EXP_IO_19	P1	IO_L58P_2			
EXP_IO_20	P8	IO_L59N_2			
EXP_IO_21	P7	IO_L59P_2			
EXP_IO_22	N4	IO_L60N_2			
EXP_IO_23	N3	IO_L60P_2			
EXP_IO_24	P3	IO_L85N_2			
EXP_IO_25	P2	IO_L85P_2			
EXP_IO_26	R8	IO_L86N_2			
EXP_IO_27	R7	IO_L86P_2			
EXP_IO_28	P5	IO_L87N_2			
EXP_IO_29	P4	IO_L87P_2			
EXP_IO_30	R2	IO_L88N_2/VREF_2			
EXP_IO_31	T2	IO_L88P_2			
EXP_IO_32	R6	IO_L89N_2			
EXP_IO_33	R5	IO_L89P_2			
EXP_IO_34	R4	IO_L90N_2			
EXP_IO_35	R3	IO_L90P_2			

NC ON P7

XC2VP_FF896

CENTER

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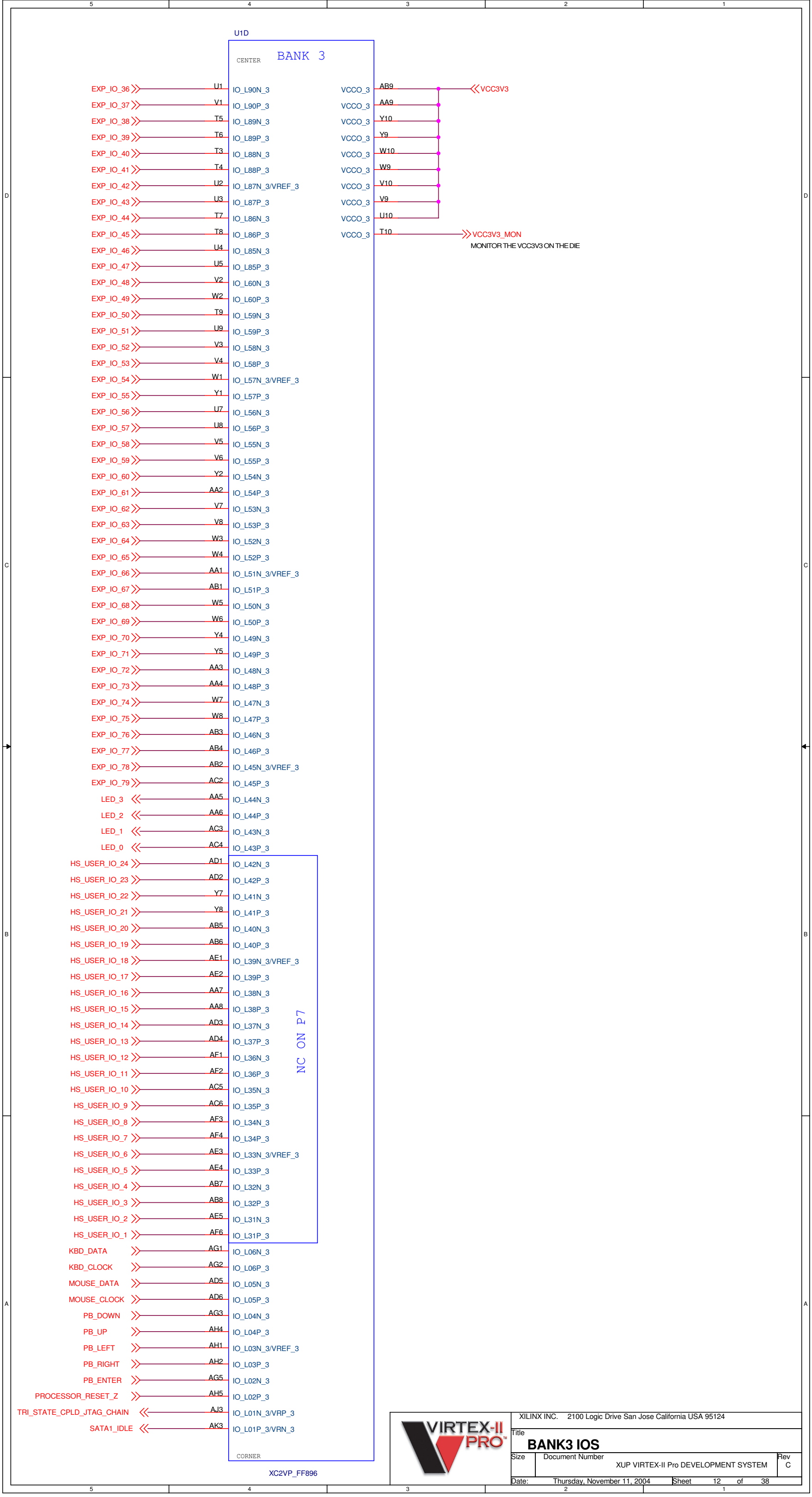
U1D
CENTER
BANK 3
EXP_IO_36 U1 IO_L90N_3
EXP_IO_37 V1 IO_L90P_3
EXP_IO_38 T5 IO_L89N_3
EXP_IO_39 T6 IO_L89P_3
EXP_IO_40 T3 IO_L88N_3
EXP_IO_41 T4 IO_L88P_3
EXP_IO_42 U2 IO_L87N_3/VREF_3
EXP_IO_43 U3 IO_L87P_3
EXP_IO_44 T7 IO_L86N_3
EXP_IO_45 T8 IO_L86P_3
EXP_IO_46 U4 IO_L85N_3
EXP_IO_47 U5 IO_L85P_3
EXP_IO_48 V2 IO_L60N_3
EXP_IO_49 W2 IO_L60P_3
EXP_IO_50 T9 IO_L59N_3
EXP_IO_51 U9 IO_L59P_3
EXP_IO_52 V3 IO_L58N_3
EXP_IO_53 V4 IO_L58P_3
EXP_IO_54 W1 IO_L57N_3/VREF_3
EXP_IO_55 Y1 IO_L57P_3
EXP_IO_56 U7 IO_L56N_3
EXP_IO_57 U8 IO_L56P_3
EXP_IO_58 V5 IO_L55N_3
EXP_IO_59 V6 IO_L55P_3
EXP_IO_60 Y2 IO_L54N_3
EXP_IO_61 AA2 IO_L54P_3
EXP_IO_62 V7 IO_L53N_3
EXP_IO_63 V8 IO_L53P_3
EXP_IO_64 W3 IO_L52N_3
EXP_IO_65 W4 IO_L52P_3
EXP_IO_66 AA1 IO_L51N_3/VREF_3
EXP_IO_67 AB1 IO_L51P_3
EXP_IO_68 W5 IO_L50N_3
EXP_IO_69 W6 IO_L50P_3
EXP_IO_70 Y4 IO_L49N_3
EXP_IO_71 Y5 IO_L49P_3
EXP_IO_72 AA3 IO_L48N_3
EXP_IO_73 AA4 IO_L48P_3
EXP_IO_74 W7 IO_L47N_3
EXP_IO_75 W8 IO_L47P_3
EXP_IO_76 AB3 IO_L46N_3
EXP_IO_77 AB4 IO_L46P_3
EXP_IO_78 AB2 IO_L45N_3/VREF_3
EXP_IO_79 AC2 IO_L45P_3
LED_3 AA5 IO_L44N_3
LED_2 AA6 IO_L44P_3
LED_1 AC3 IO_L43N_3
LED_0 AC4 IO_L43P_3
HS_USER_IO_24 AD1 IO_L42N_3
HS_USER_IO_23 AD2 IO_L42P_3
HS_USER_IO_22 Y7 IO_L41N_3
HS_USER_IO_21 Y8 IO_L41P_3
HS_USER_IO_20 AB5 IO_L40N_3
HS_USER_IO_19 AB6 IO_L40P_3
HS_USER_IO_18 AE1 IO_L39N_3/VREF_3
HS_USER_IO_17 AE2 IO_L39P_3
HS_USER_IO_16 AA7 IO_L38N_3
HS_USER_IO_15 AA8 IO_L38P_3
HS_USER_IO_14 AD3 IO_L37N_3
HS_USER_IO_13 AD4 IO_L37P_3
HS_USER_IO_12 AF1 IO_L36N_3
HS_USER_IO_11 AF2 IO_L36P_3
HS_USER_IO_10 AC5 IO_L35N_3
HS_USER_IO_9 AC6 IO_L35P_3
HS_USER_IO_8 AF3 IO_L34N_3
HS_USER_IO_7 AF4 IO_L34P_3
HS_USER_IO_6 AE3 IO_L33N_3/VREF_3
HS_USER_IO_5 AE4 IO_L33P_3
HS_USER_IO_4 AB7 IO_L32N_3
HS_USER_IO_3 AB8 IO_L32P_3
HS_USER_IO_2 AE5 IO_L31N_3
HS_USER_IO_1 AF6 IO_L31P_3
NC ON P7
KBD_DATA AG1 IO_L06N_3
KBD_CLOCK AG2 IO_L06P_3
MOUSE_DATA AD5 IO_L05N_3
MOUSE_CLOCK AD6 IO_L05P_3
PB_DOWN AG3 IO_L04N_3
PB_UP AH4 IO_L04P_3
PB_LEFT AH1 IO_L03N_3/VREF_3
PB_RIGHT AH2 IO_L03P_3
PB_ENTER AG5 IO_L02N_3
PROCESSOR_RESET_Z AH5 IO_L02P_3
TRI_STATE_CPLD_JTAG_CHAIN AJ3 IO_L01N_3/VRP_3
SATA1_IDLE AK3 IO_L01P_3/VRN_3
CORNER
XC2VP_FF896
VCCO_3 AB9
VCCO_3 AA9
VCCO_3 Y10
VCCO_3 Y9
VCCO_3 W10
VCCO_3 W9
VCCO_3 V10
VCCO_3 V9
VCCO_3 U10
VCCO_3 T10
VCC3V3
VCC3V3_MON
MONITOR THE VCC3V3 ON THE DIE
VIRTEX-II PRO
XILINX INC. 2100 Logic Drive San Jose California USA 95124
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BANK3 IOS
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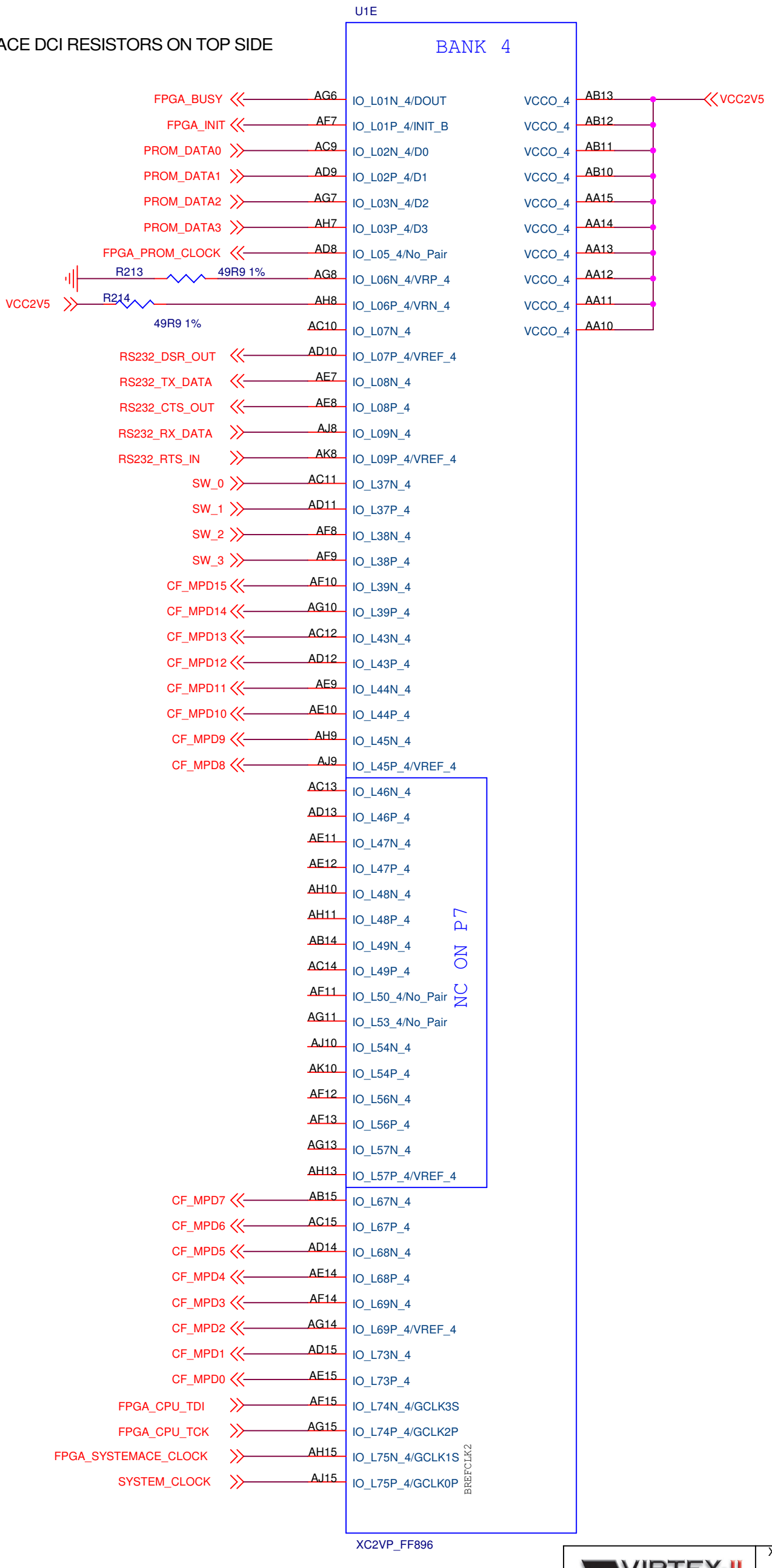
PLACE DCI RESISTORS ON TOP SIDE



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Title **BANK4 IOS**

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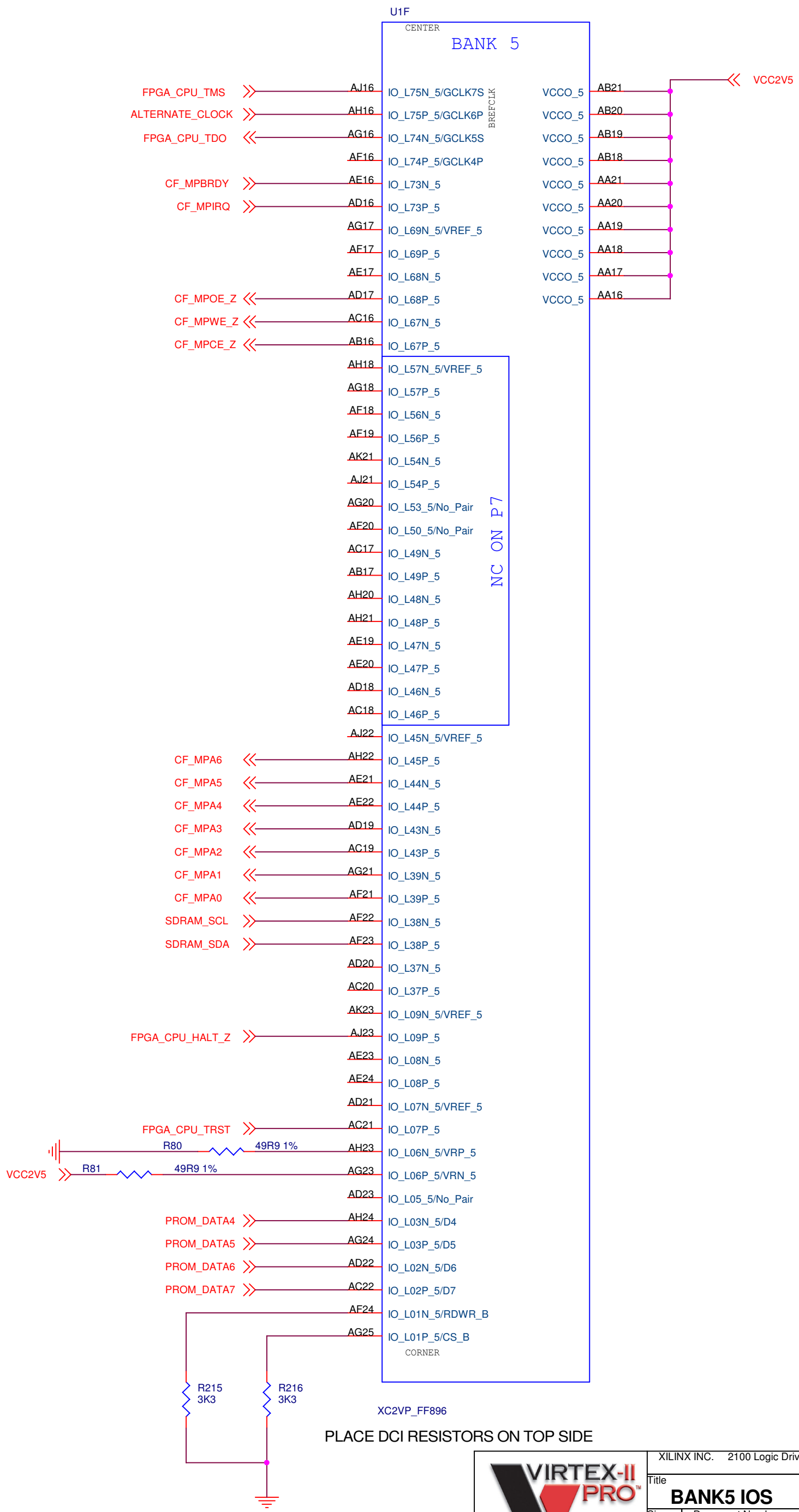

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title
BANK5 IOS

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev C

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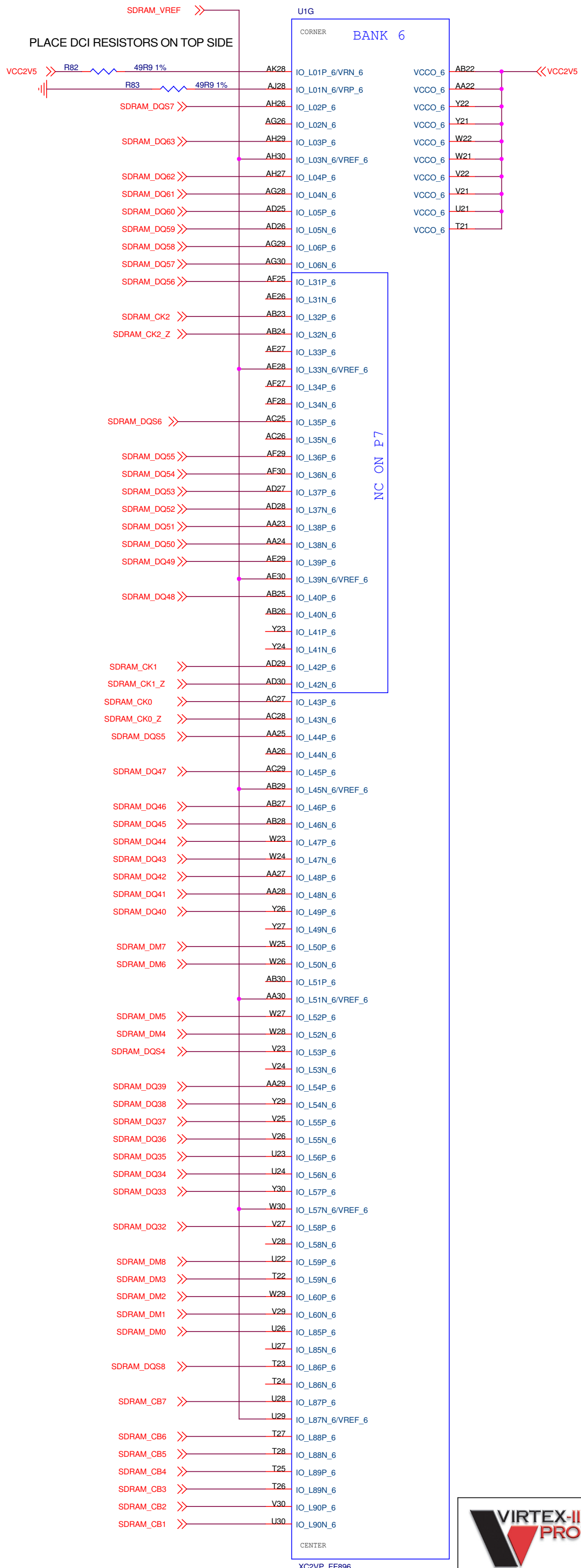
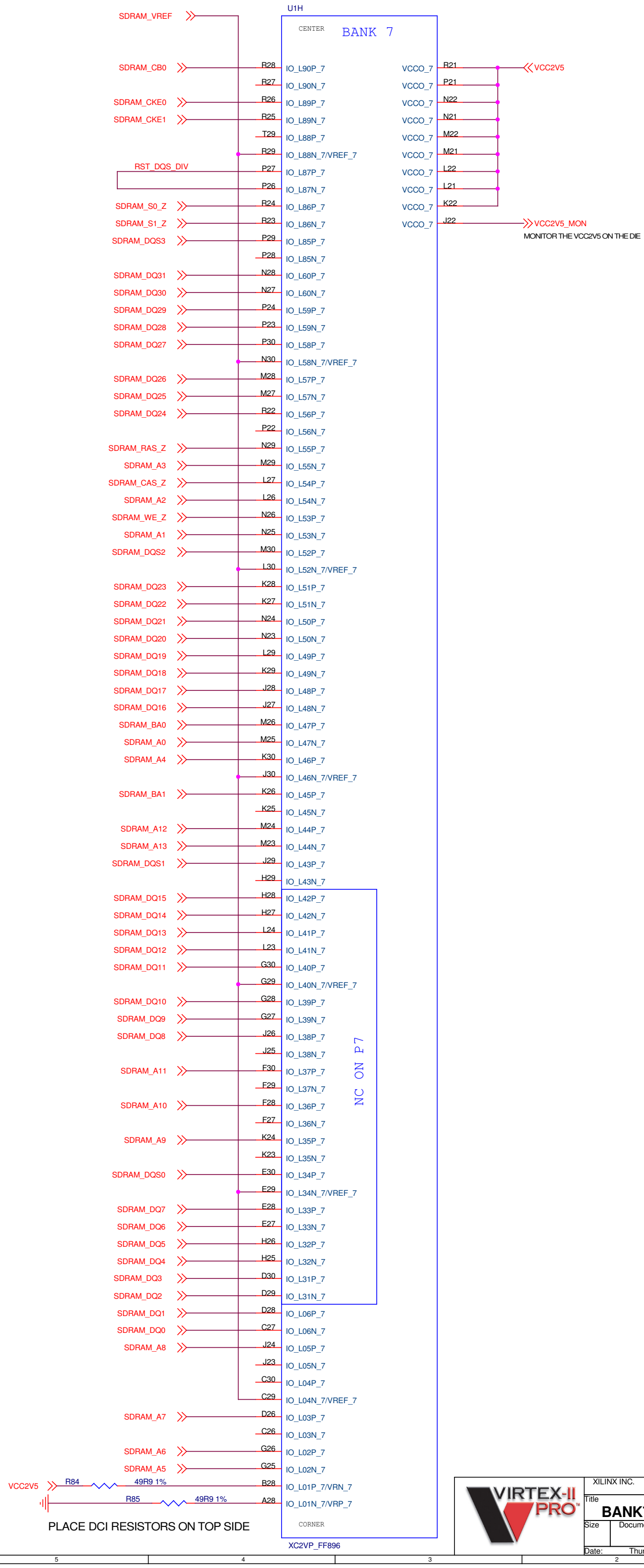


XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title
BANK6 IOS

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

Date: Thursday, November 11, 2004 Sheet 15 of 38



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Title
BANK7 IOS

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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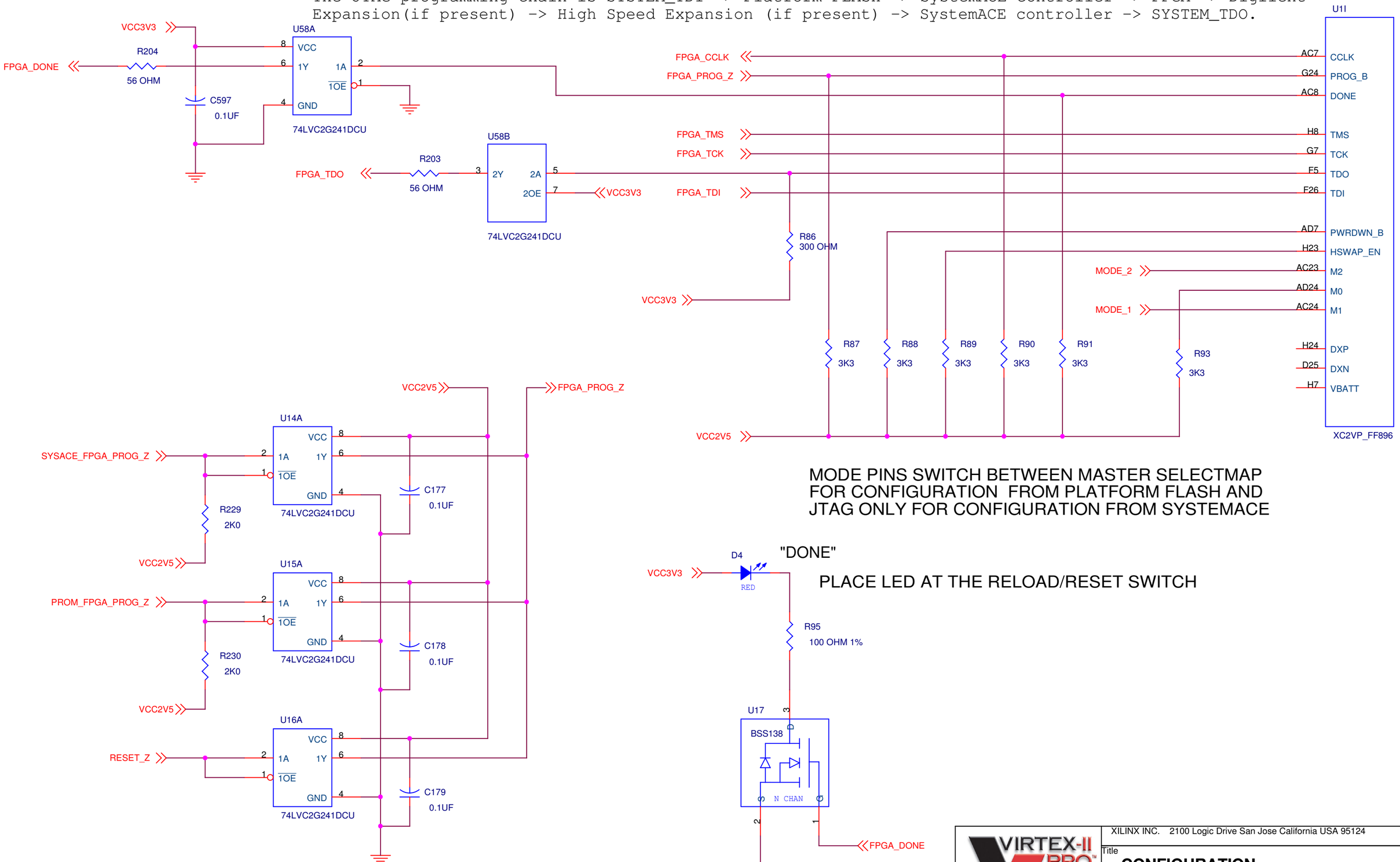
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.



MODE PINS SWITCH BETWEEN MASTER SELECTMAP FOR CONFIGURATION FROM PLATFORM FLASH AND JTAG ONLY FOR CONFIGURATION FROM SYSTEMACE

PLACE LED AT THE RELOAD/RESET SWITCH

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Title: **CONFIGURATION**

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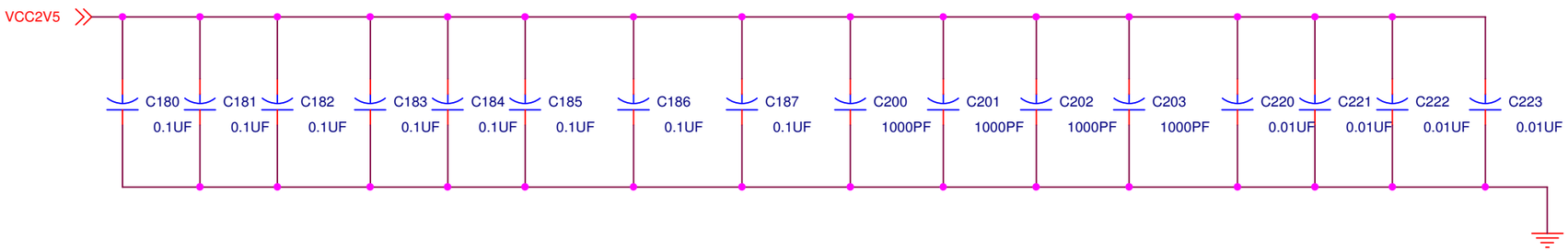

DISTRIBUTE CAPS EVENLY ON ALL BANKS

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Title

FPGA VAUX CAPS

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DISTRIBUTE CAPS EVENLY ON ALL BANKS

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Title

FPGA VCCO CAPS

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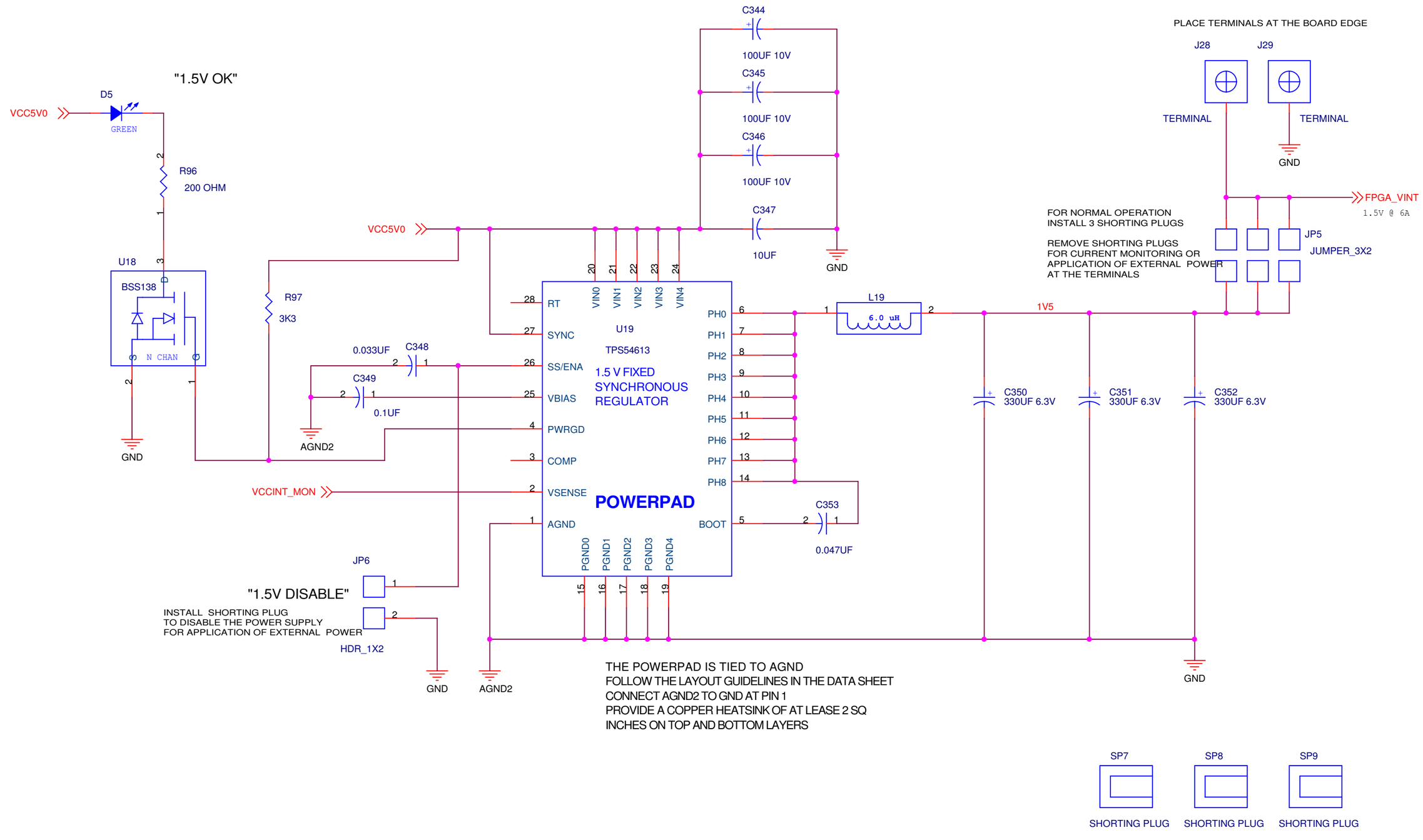

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Title **FPGA VINT**

Size	Document Number	Rev
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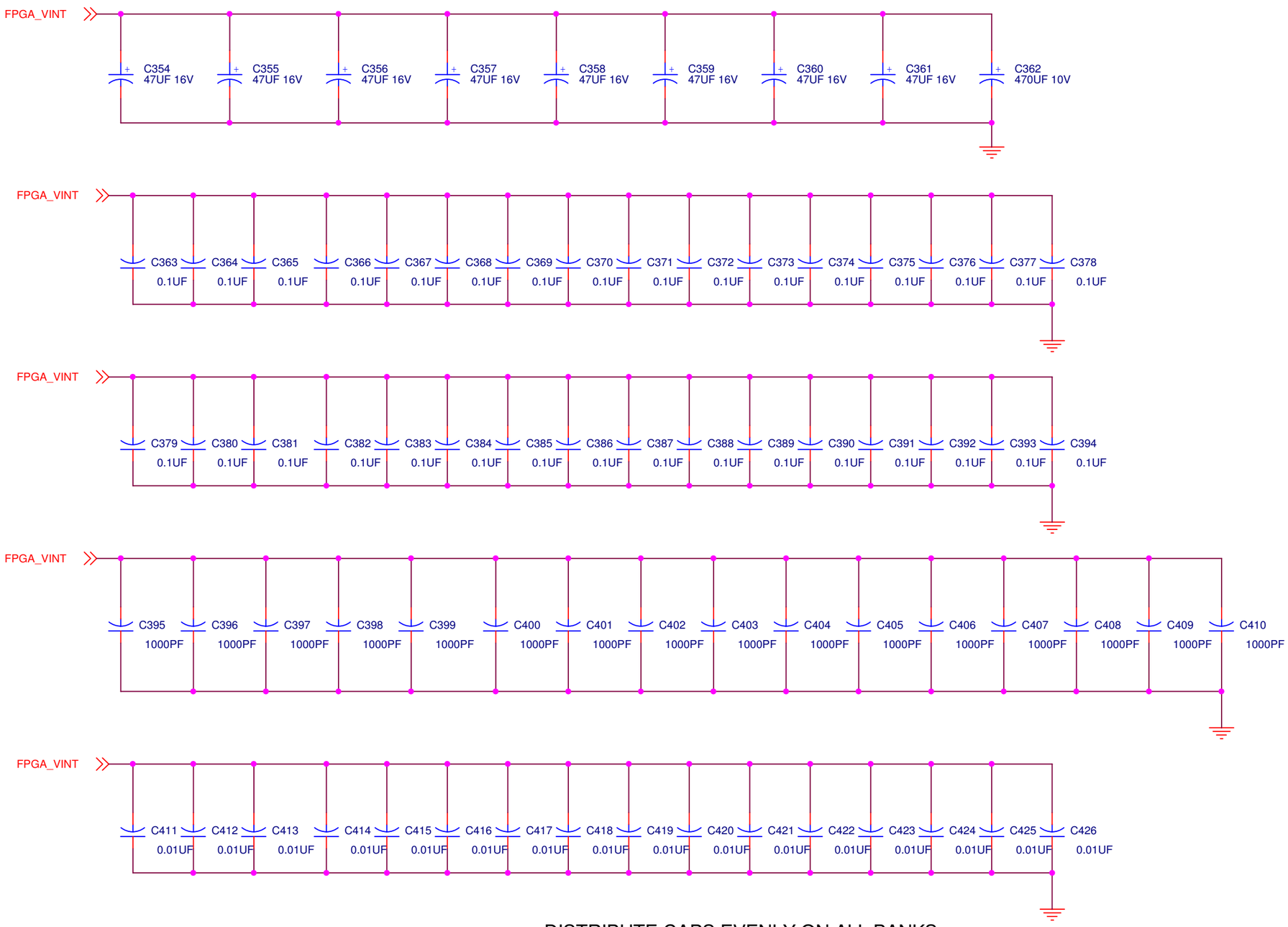

DISTRIBUTE CAPS EVENLY ON ALL BANKS

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Title

FPGA VINT CAPS

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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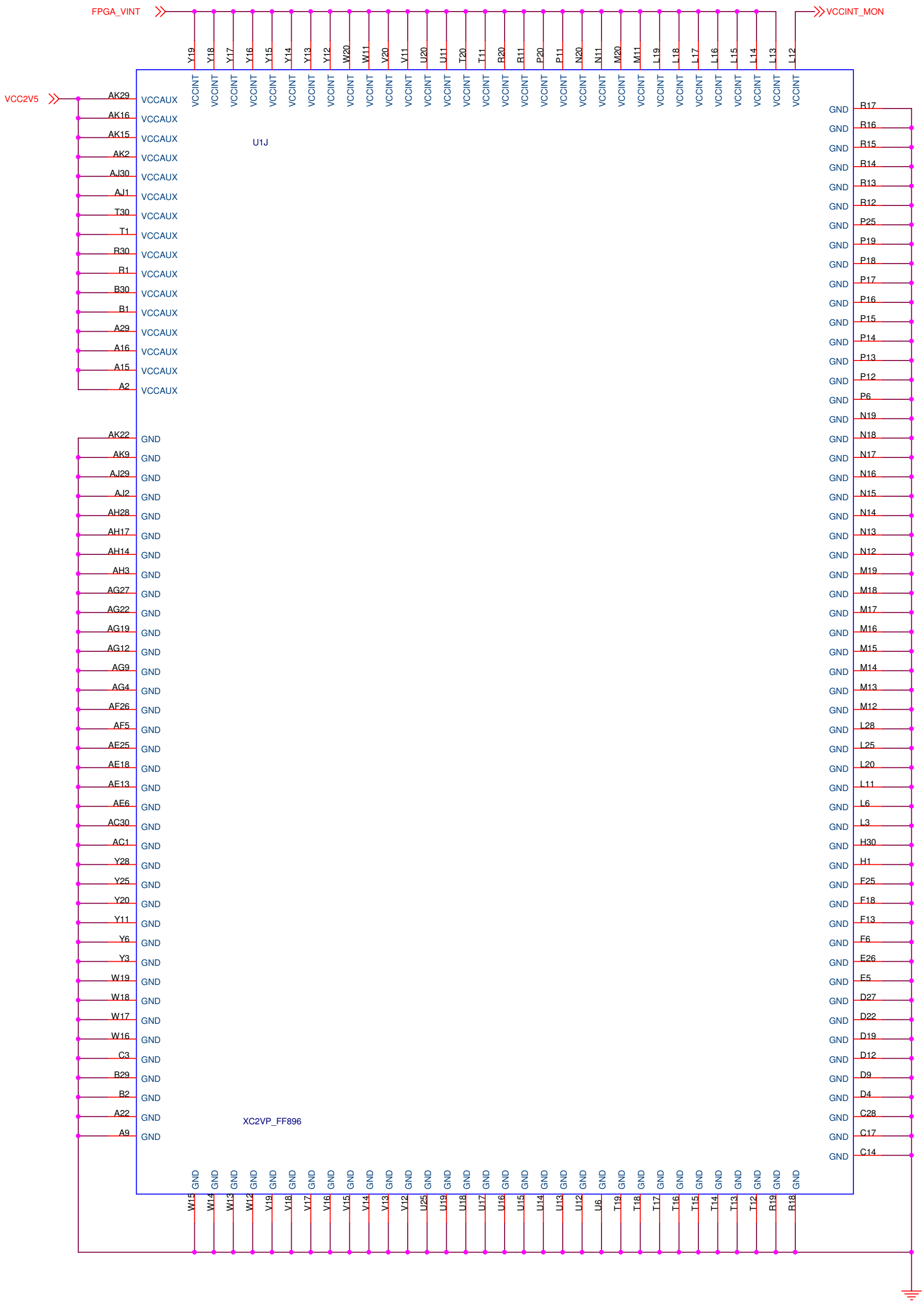

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Title

FPGA 0 VINT VAUX GND

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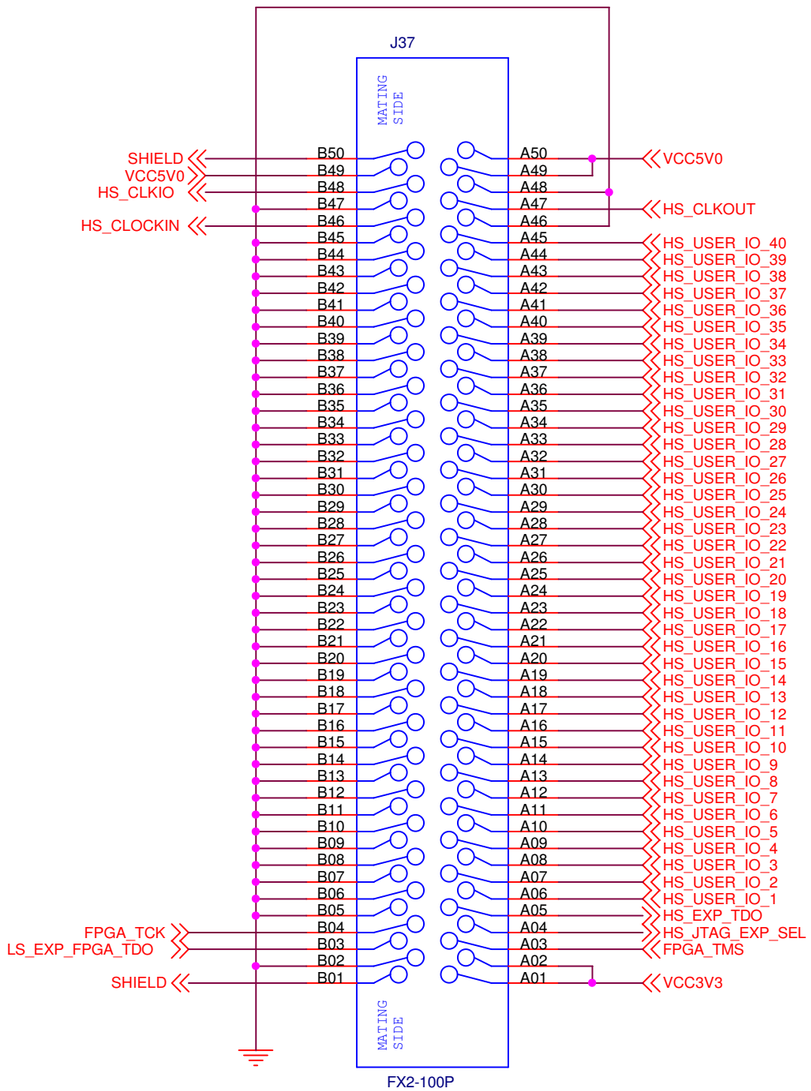
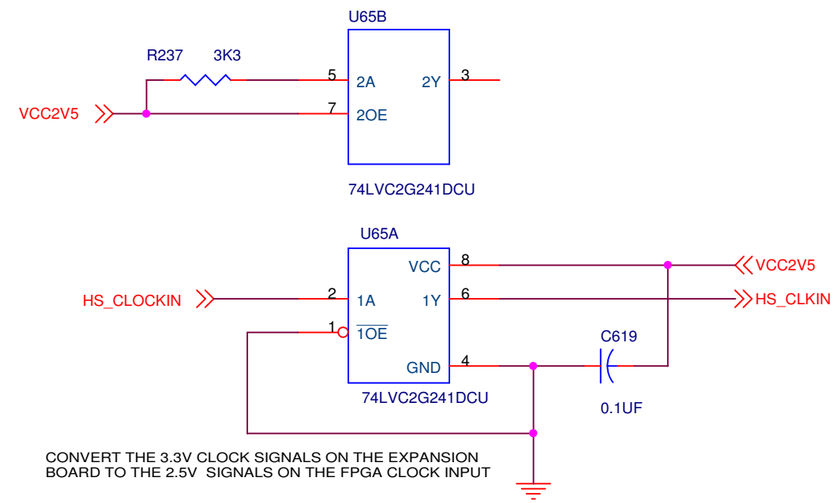
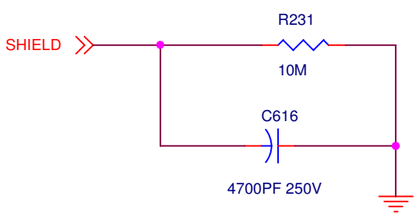
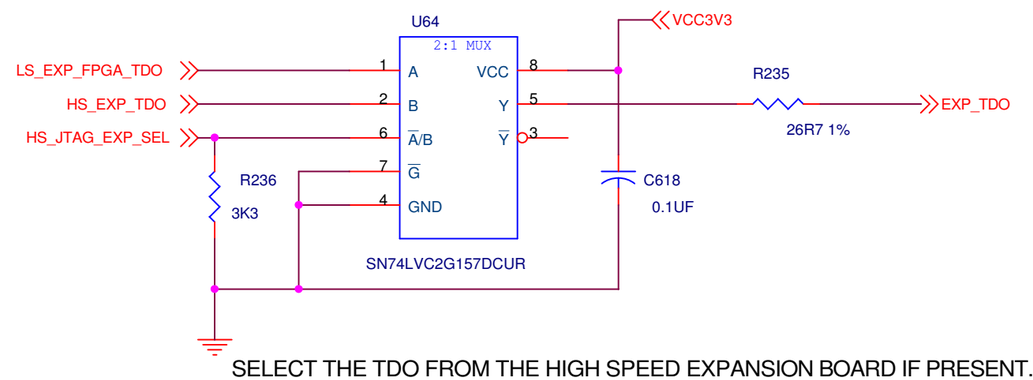
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.









SELECT THE TDO FROM THE HIGH SPEED EXPANSION BOARD IF PRESENT. THE EXPANSION BOARD WILL PULL UP HS_JTAG_EXP_SEL.

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Title
HIGH SPEED EXPANSION PORT

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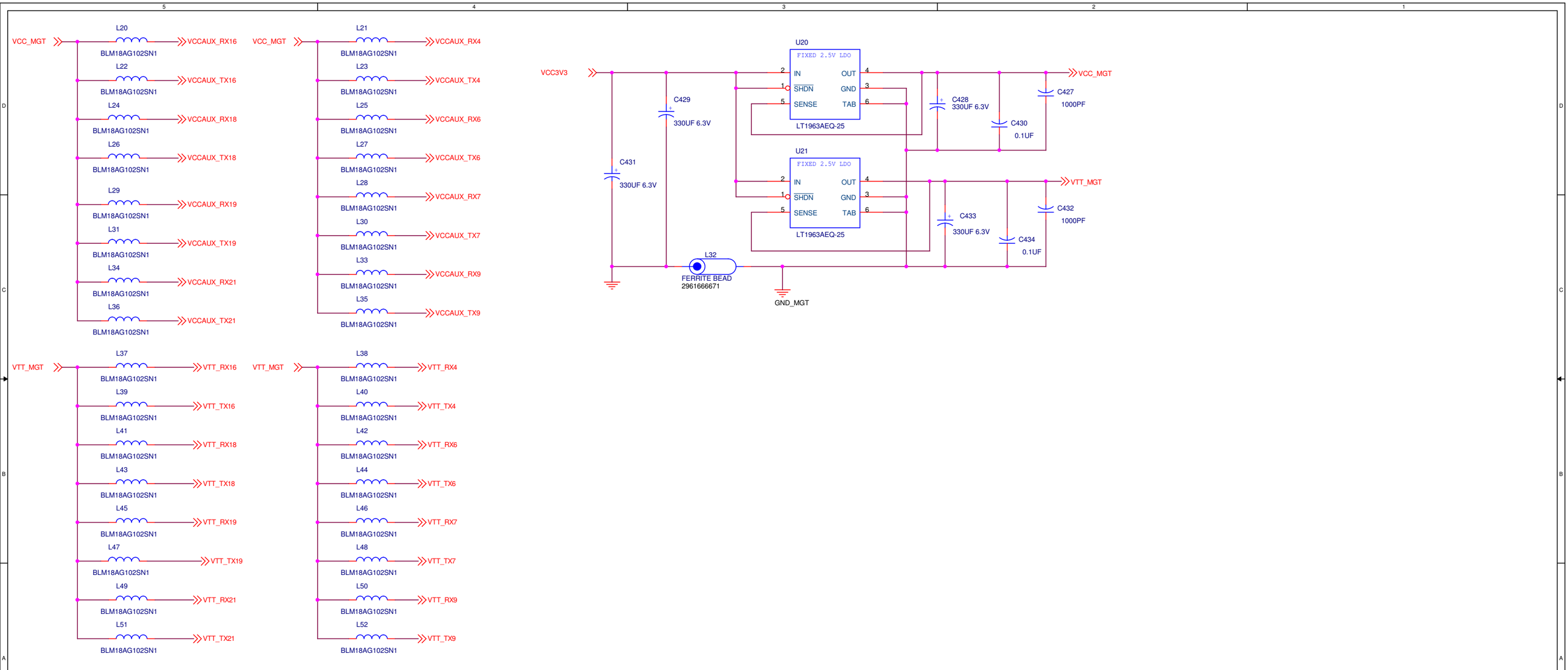
SDRAM NET LENGTH MATCHING

SIGNAL GROUP	MIN LENGTH	MAX LENGTH	NOTES
Command to Clock SDRAM_A[13:0] to SDRAM_CKn SDRAM_DM[7:0] to SDRAM_CKn SDRAM_RAS_Z to SDRAM_CKn SDRAM_CAS_Z to SDRAM_CKn SDRAM_WE_Z to SDRAM_CKn SDRAM_BA0 to SDRAM_CKn SDRAM_BA1 to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) - 0.5"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge)
Control to Clock SDRAM_CKE0 to SDRAM_CKn SDRAM_CKE1 to SDRAM_CKn SDRAM_S0_Z to SDRAM_CKn SDRAM_S1_Z to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) - 0.5"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge)
Strobe to Clock SDRAM_DQS8 to SDRAM_CKn SDRAM_DQS7 to SDRAM_CKn SDRAM_DQS6 to SDRAM_CKn SDRAM_DQS5 to SDRAM_CKn SDRAM_DQS4 to SDRAM_CKn SDRAM_DQS3 to SDRAM_CKn SDRAM_DQS2 to SDRAM_CKn SDRAM_DQS1 to SDRAM_CKn SDRAM_DQS0 to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) + 1"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 15 mils (edge to edge)
Data to Strobe SDRAM_CB[7:0] to SDRAM_DQS8 SDRAM_DQ[63:56] to SDRAM_DQS7 SDRAM_DQ[55:48] to SDRAM_DQS6 SDRAM_DQ[47:40] to SDRAM_DQS5 SDRAM_DQ[39:32] to SDRAM_DQS4 SDRAM_DQ[31:24] to SDRAM_DQS3 SDRAM_DQ[23:16] to SDRAM_DQS2 SDRAM_DQ[15:8] to SDRAM_DQS1 SDRAM_DQ[7:0] to SDRAM_DQS0	SDRAM_DQS8 - 25 mils SDRAM_DQS7 - 25 mils SDRAM_DQS6 - 25 mils SDRAM_DQS5 - 25 mils SDRAM_DQS4 - 25 mils SDRAM_DQS3 - 25 mils SDRAM_DQS2 - 25 mils SDRAM_DQS1 - 25 mils SDRAM_DQS0 - 25 mils	SDRAM_DQS8 + 25 mils SDRAM_DQS7 + 25 mils SDRAM_DQS6 + 25 mils SDRAM_DQS5 + 25 mils SDRAM_DQS4 + 25 mils SDRAM_DQS3 + 25 mils SDRAM_DQS2 + 25 mils SDRAM_DQS1 + 25 mils SDRAM_DQS0 + 25 mils	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge) MINIMUM TRACE LENGTH 1.5"
Differential Clock Length SDRAM_CK0_Z to SDRAM_CK0 SDRAM_CK1_Z to SDRAM_CK1 SDRAM_CK2_Z to SDRAM_CK2	SDRAM_CK0 - 10 mils SDRAM_CK1 - 10 mils SDRAM_CK2 - 10 mils	SDRAM_CK0 + 10 mils SDRAM_CK1 + 10 mils SDRAM_CK2 + 10 mils	ROUTE AS 100 OHM DIFFERENTIAL MIN SPACING TO OTHER SDRAM SIGNALS 20 mils MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 8 mils TRACE SPACING 5 mils (edge to edge)
Clock to Clock Length SDRAM_CKm to SDRAM_CKn SDRAM_CLOCK_FEEDBACK_LOOP	SDRAM_CKn - 20 mils	SDRAM_CKn + 20 mils	MINIMUM TRACE LENGTH 3.5"

SIGNAL GROUP	MIN LENGTH	MAX LENGTH	NOTES
Differential Net Lengths MGT_CLK_N to MGT_CLK_P EXTERNAL_CLOCK_N to EXTERNAL_CLOCK_P MGT_TXN to MGT_TXP MGT_RXN to MGT_RXP SATA_PRT0_TXN to SATA_PRT0_TXP SATA_PRT0_RXN to SATA_PRT0_RXP SATA_PRT1_TXN to SATA_PRT1_TXP SATA_PRT1_RXN to SATA_PRT1_RXP SATA_PRT2_TXN to SATA_PRT2_TXP SATA_PRT2_RXN to SATA_PRT2_RXP SATA_PORT0_TXN to SATA_PORT0_TXP SATA_PORT1_TXN to SATA_PORT1_TXP SATA_PORT2_TXN to SATA_PORT2_TXP	MGT_CLK_P - 10 mils EXTERNAL_CLOCK_P - 10 mils MGT_TXP - 10 mils MGT_RXP - 10 mils SATA_PRT0_TXP - 10 mils SATA_PRT0_RXP - 10 mils SATA_PRT1_TXP - 10 mils SATA_PRT1_RXP - 10 mils SATA_PRT2_TXP - 10 mils SATA_PRT2_RXP - 10 mils SATA_PORT0_TXP - 10 mils SATA_PORT1_TXP - 10 mils SATA_PORT2_TXP - 10 mils	MGT_CLK_P + 10 mils EXTERNAL_CLOCK_P + 10 mils MGT_TXP + 10 mils MGT_RXP + 10 mils SATA_PRT0_TXP + 10 mils SATA_PRT0_RXP + 10 mils SATA_PRT1_TXP + 10 mils SATA_PRT1_RXP + 10 mils SATA_PRT2_TXP + 10 mils SATA_PRT2_RXP + 10 mils SATA_PORT0_TXP + 10 mils SATA_PORT1_TXP + 10 mils SATA_PORT2_TXP + 10 mils	ROUTE AS 100 OHM DIFFERENTIAL MIN SPACING TO OTHER SIGNALS 20 mils TRACE WIDTH 8 mils TRACE SPACING 5 mils (edge to edge) INCLUDE THE "R", "C" and FPGA ballout lengths



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Title: **MGT FILTERS & POWER**

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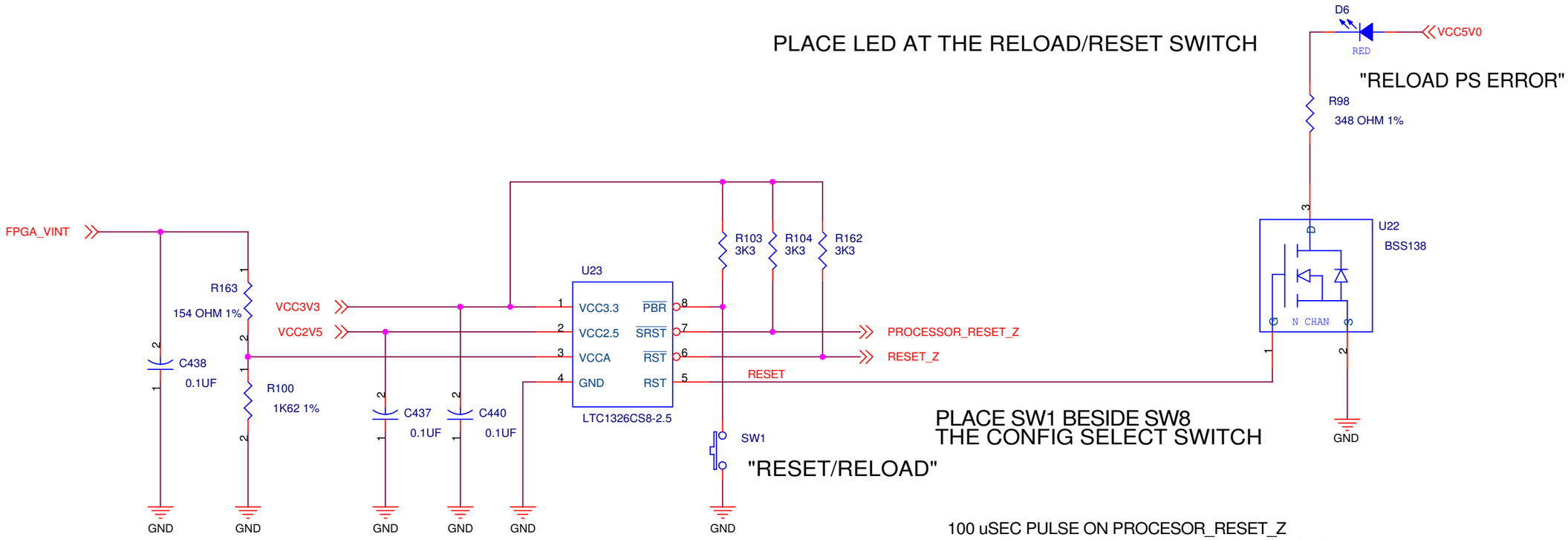
PLACE LED AT THE RELOAD/RESET SWITCH

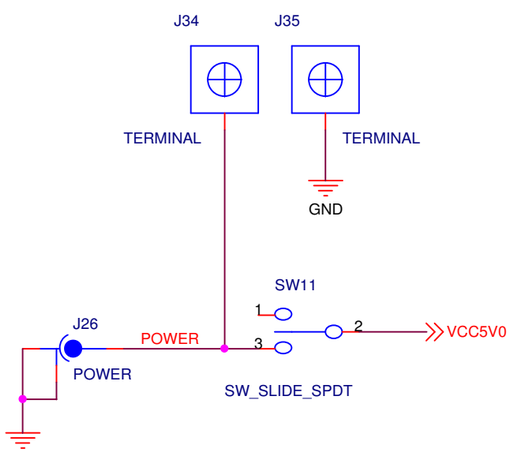


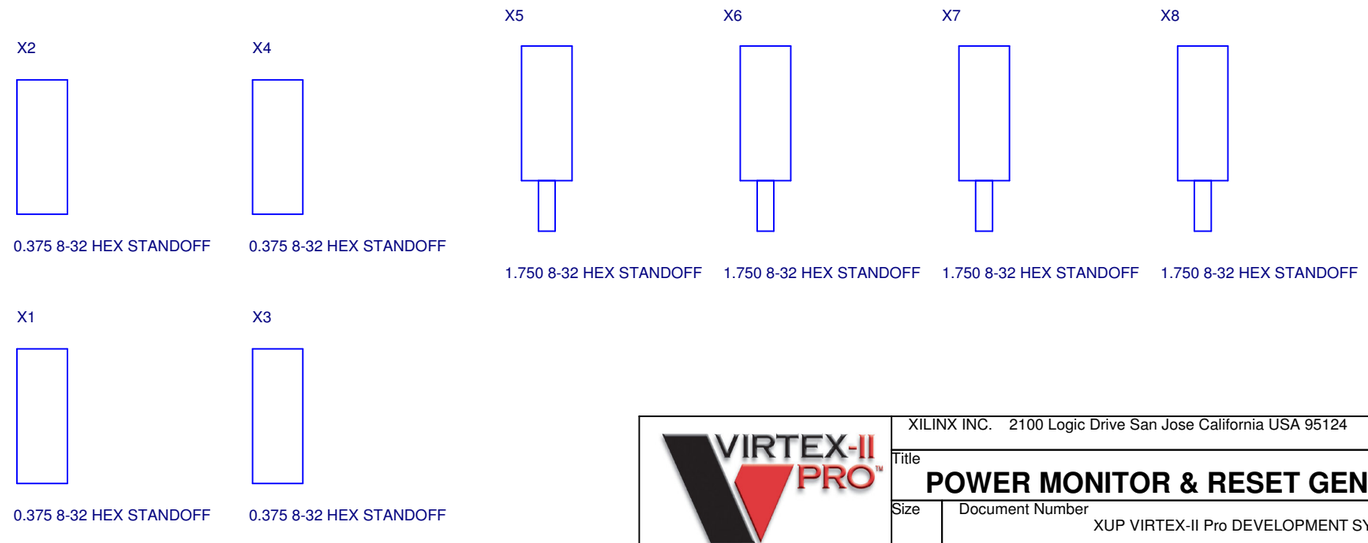
PLACE SW1 BESIDE SW8
THE CONFIG SELECT SWITCH

100 uSEC PULSE ON PROCESOR_RESET_Z
WHEN SW1 IS PRESSED FOR LESS THAN 2 SEC.

200 mSEC PULSE ON RESET_Z ON POWER UP
OR WHEN SW1 IS PRESSED FOR MORE THAN 2
SEC.

PLACE TERMINALS AT THE BOARD EDGE





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Title
POWER MONITOR & RESET GENERATION

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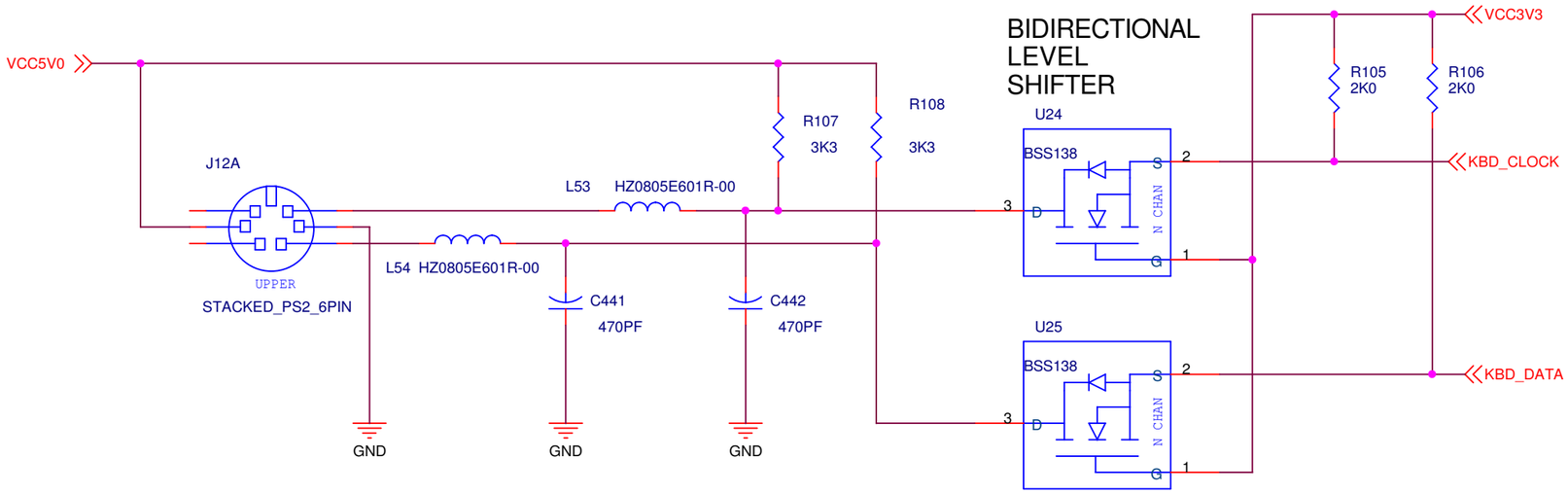

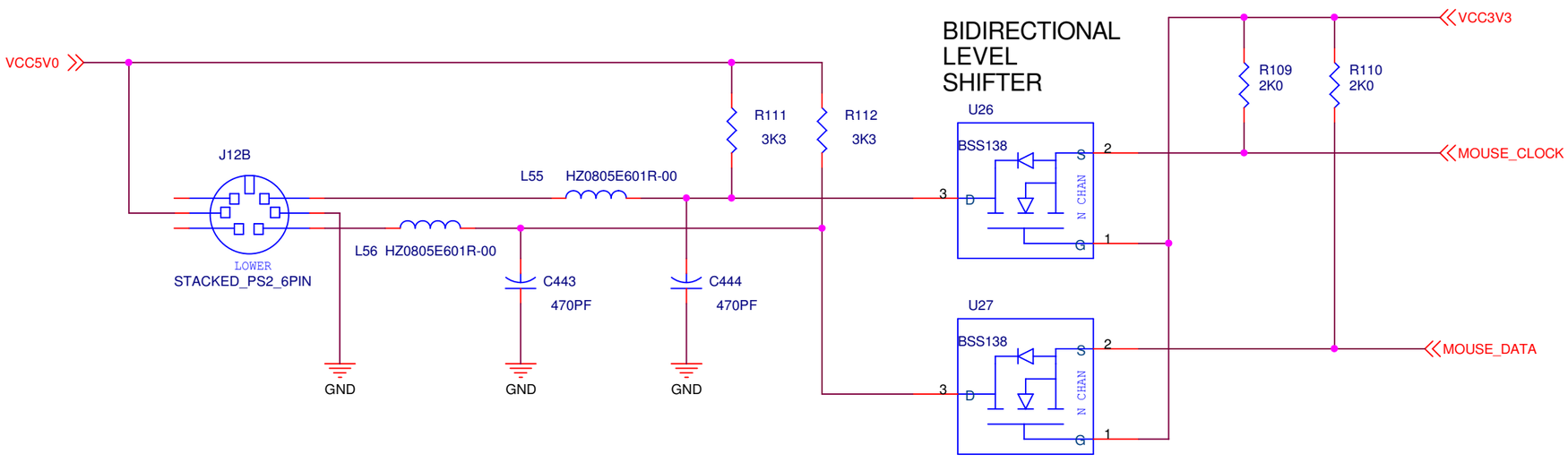

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Title
PS/2 PORTS

Size	Document Number	Rev
B	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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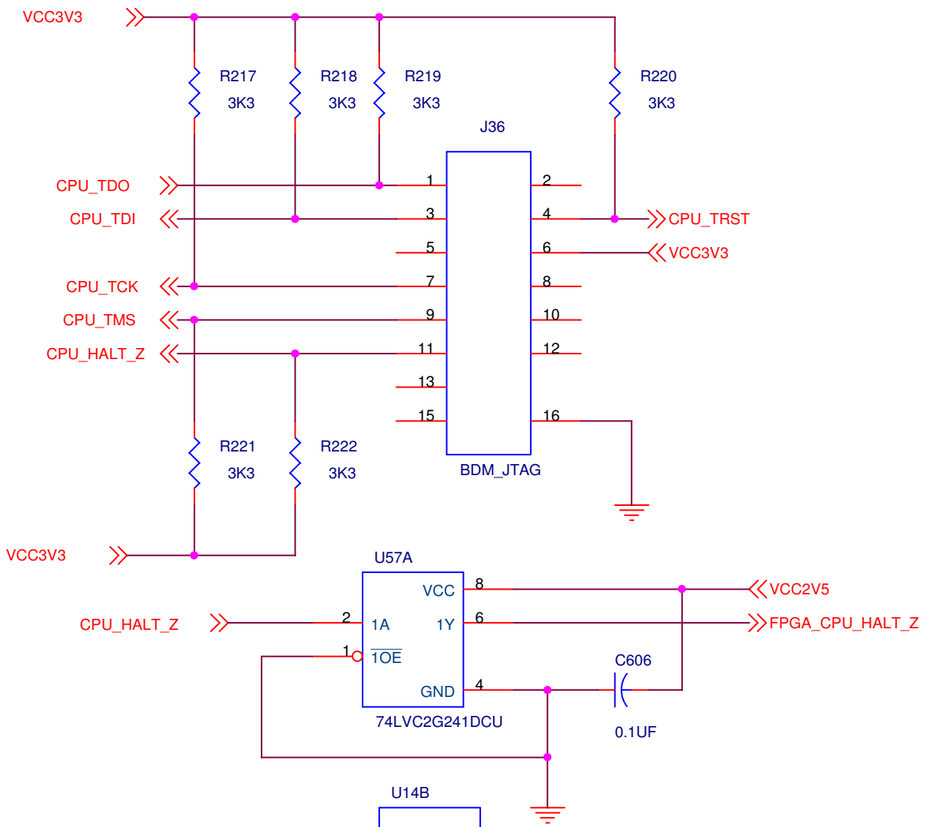

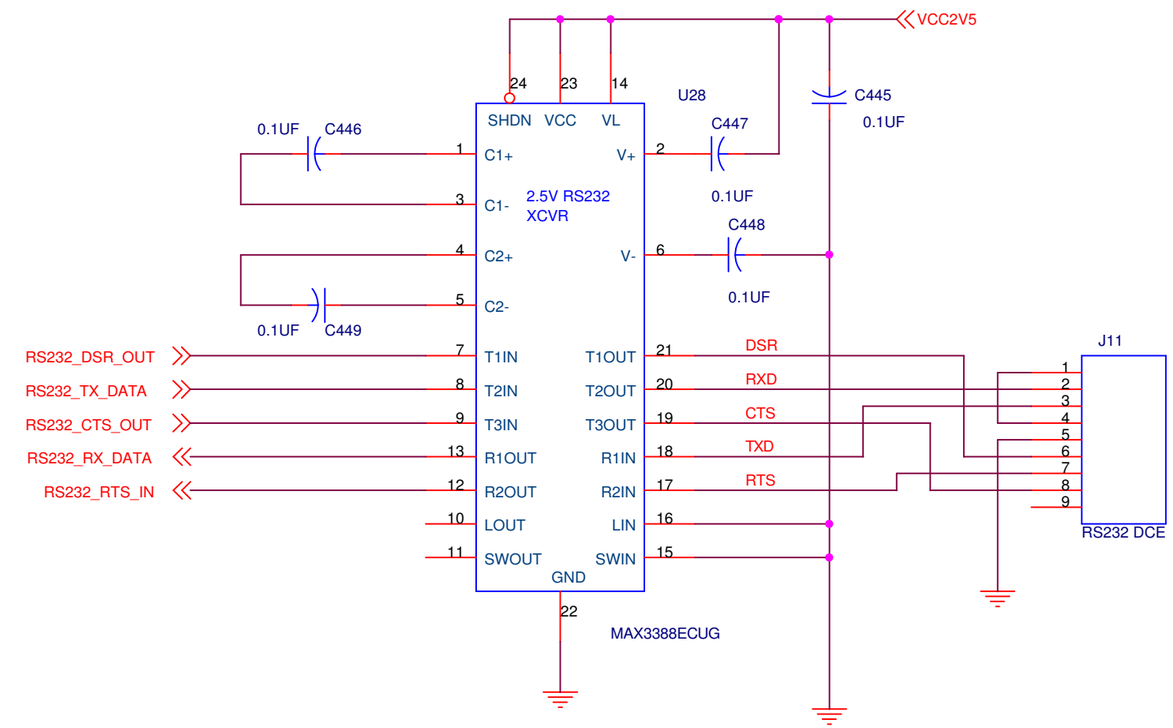

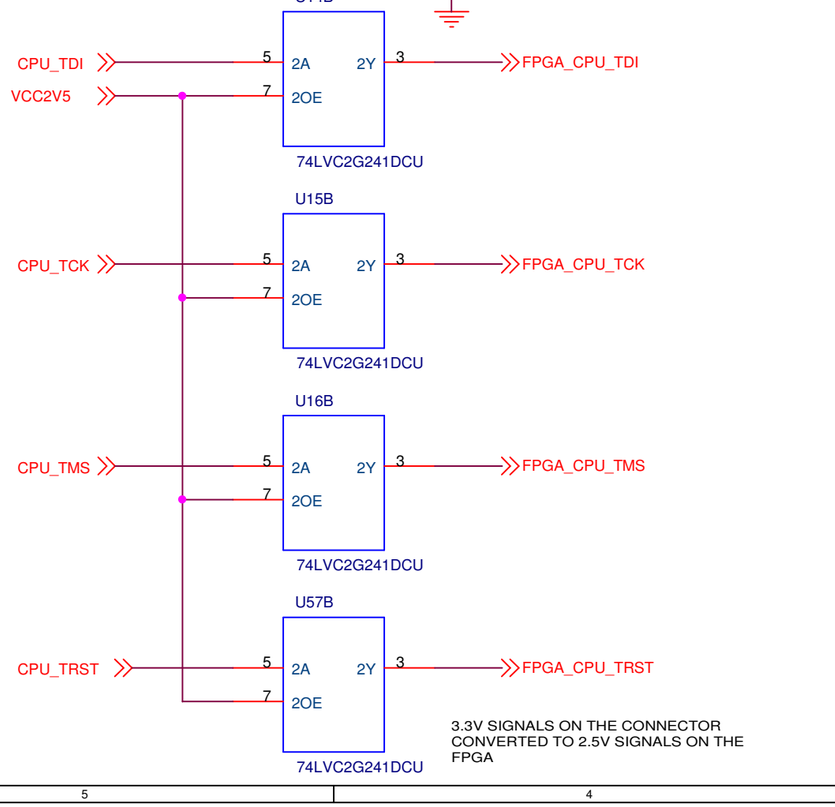

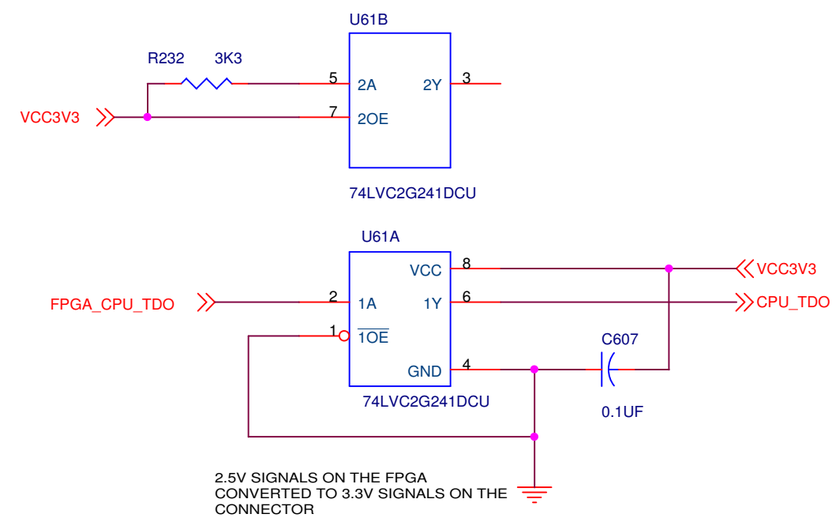

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Title

SERIAL PORT & DEBUG PORT

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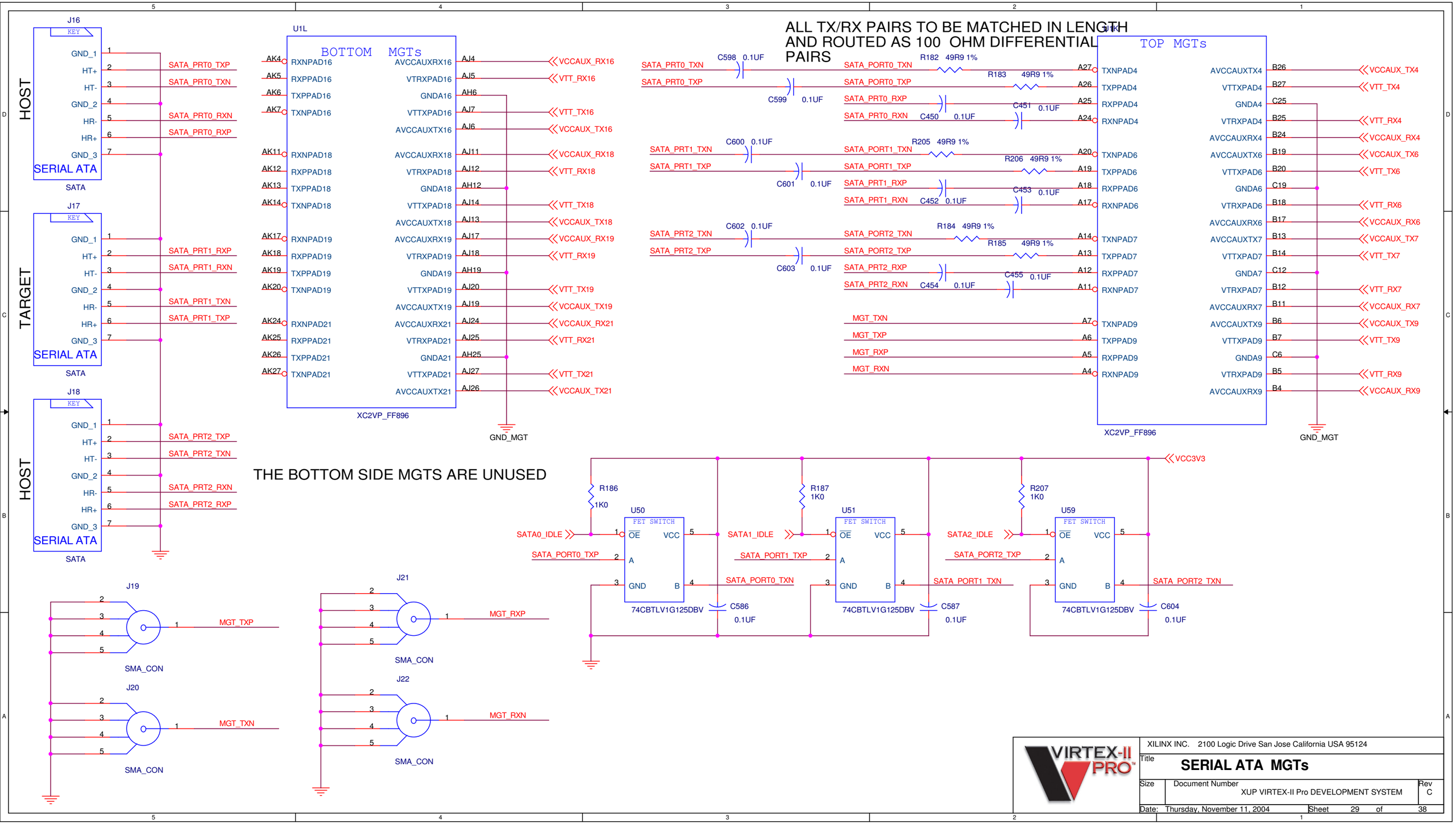

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Title: **SERIAL ATA MGTs**

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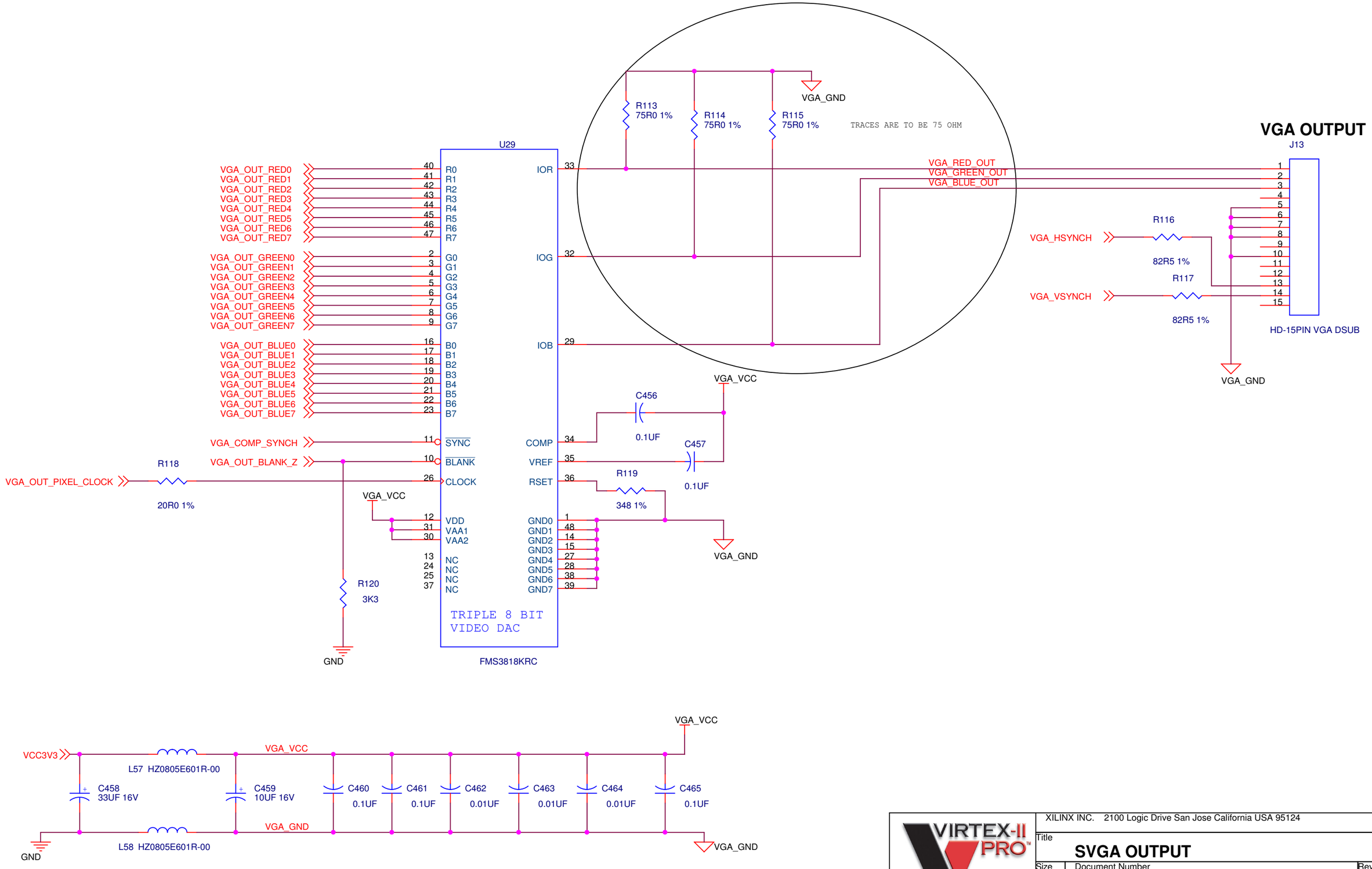

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Title: **SVGA OUTPUT**

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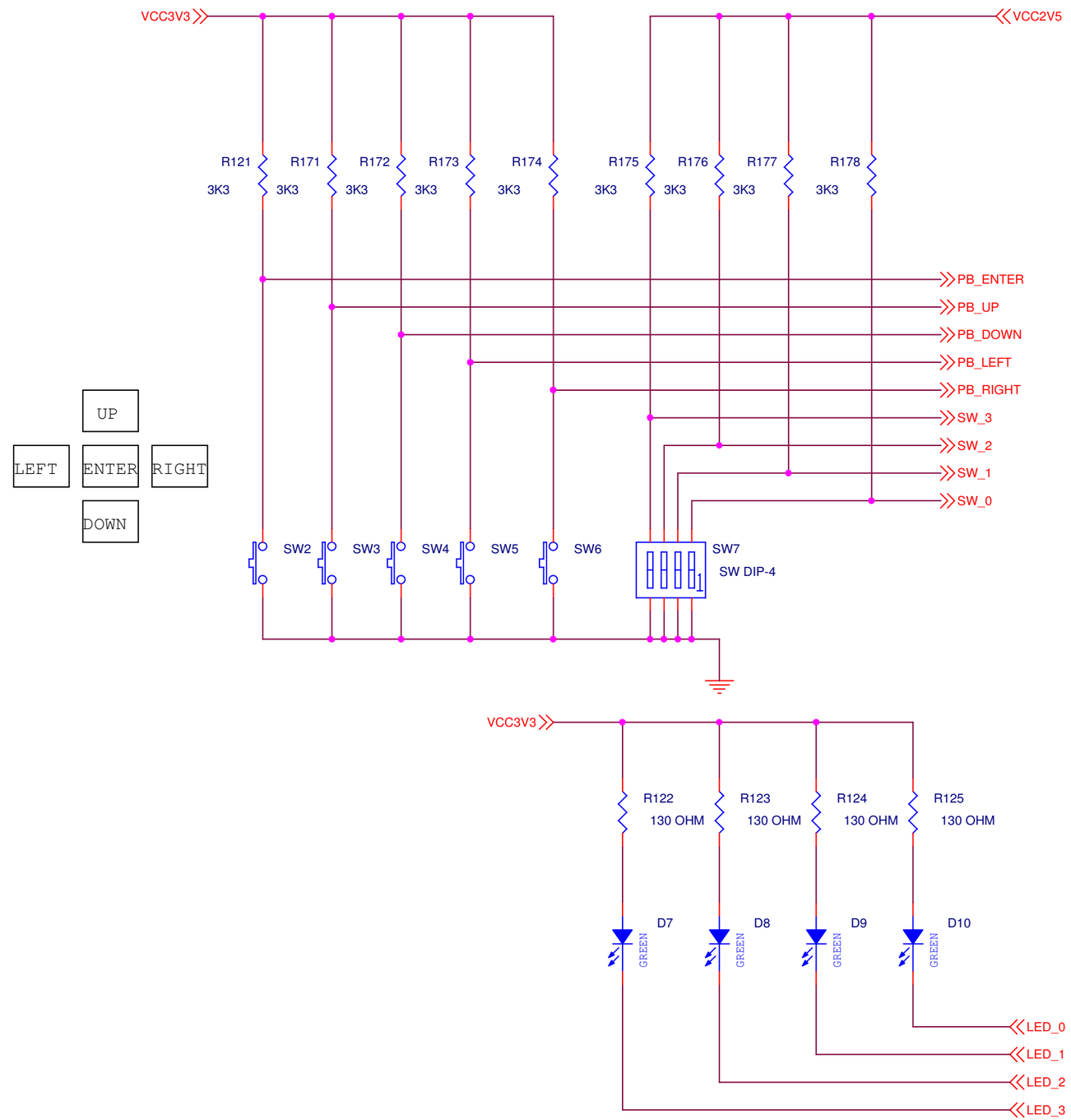

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Title
SWITCHES & LEDS

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B	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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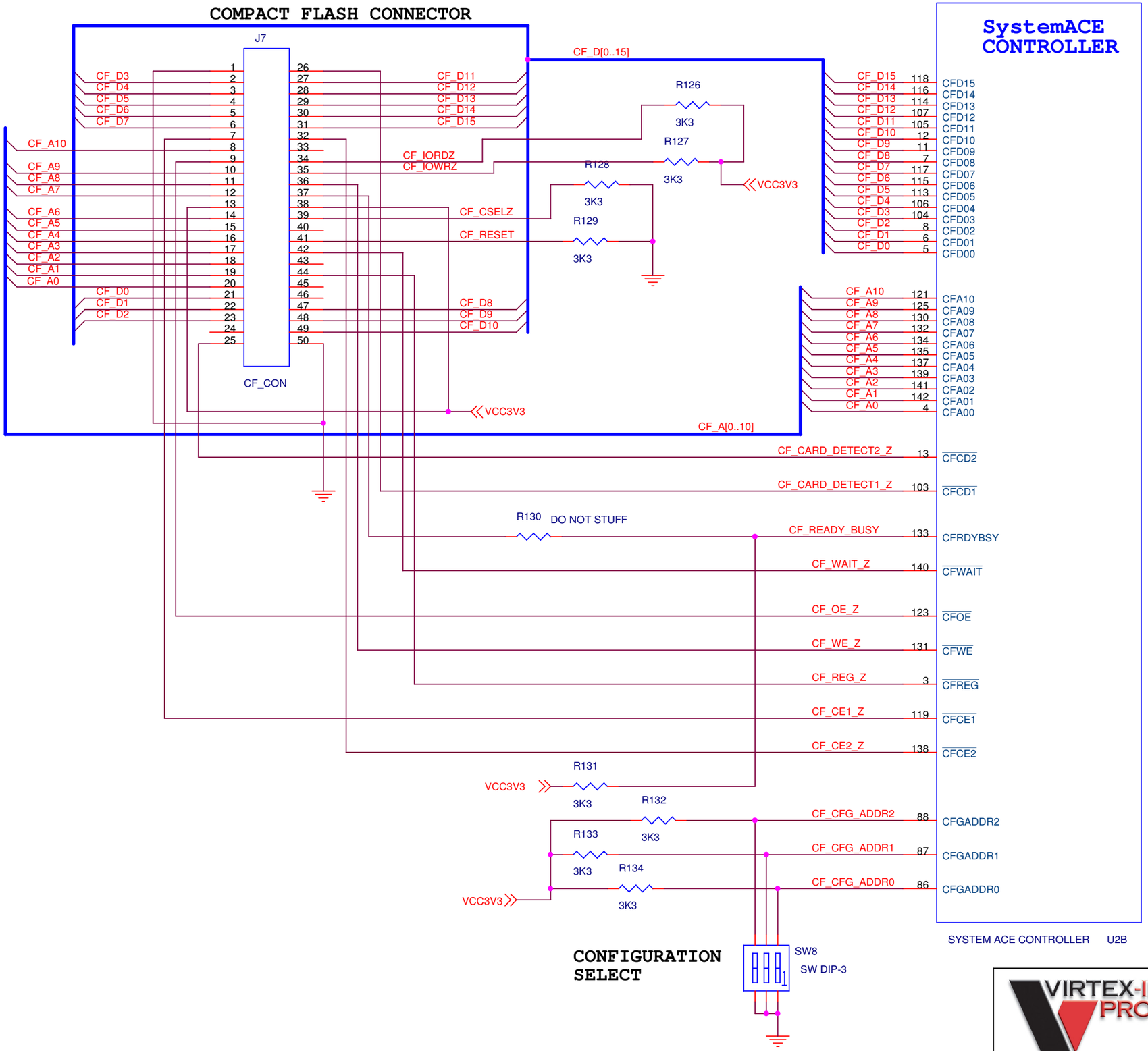

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Title: **SYSTEMACE COMPACT FLASH PORT**

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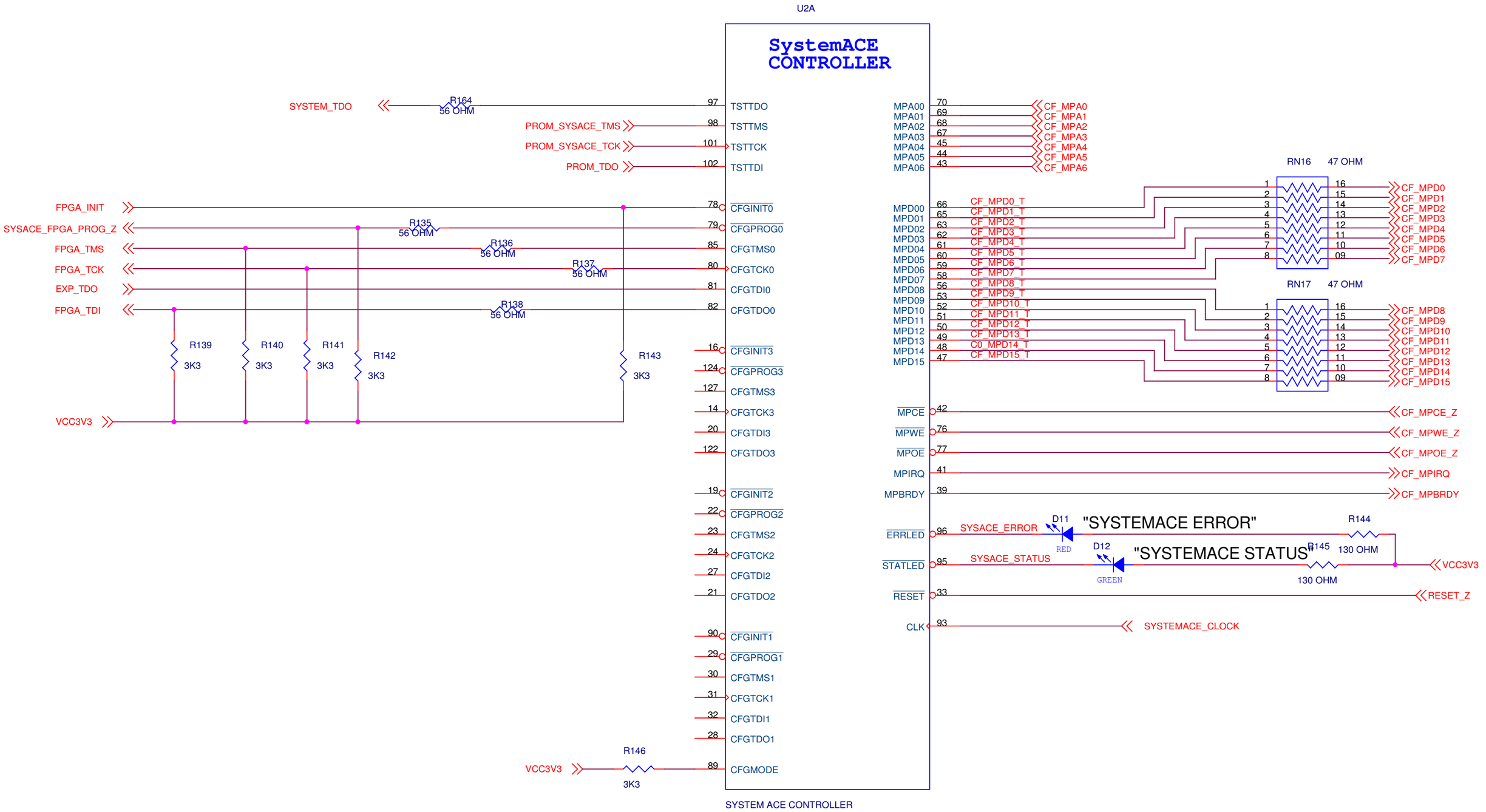
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.



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Title
SYSTEMACE MICRO PORT & JTAG TEST PORT

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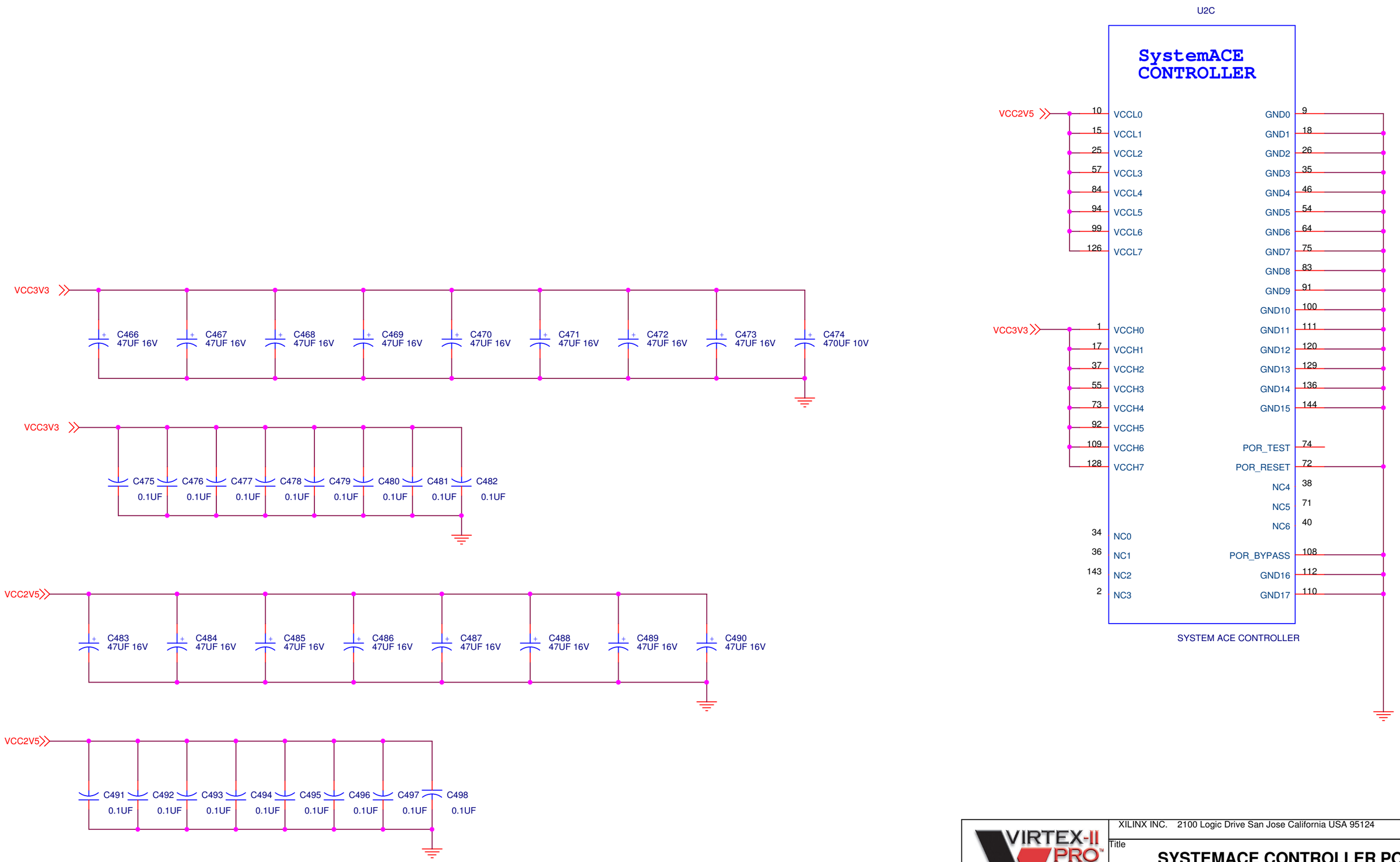

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Title: **SYSTEMACE CONTROLLER POWER**

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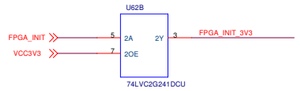
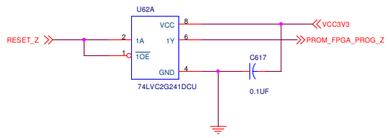
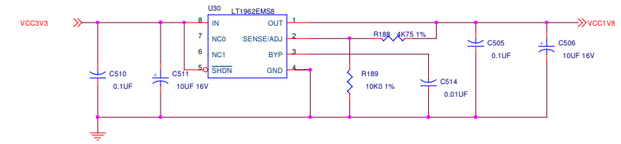
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

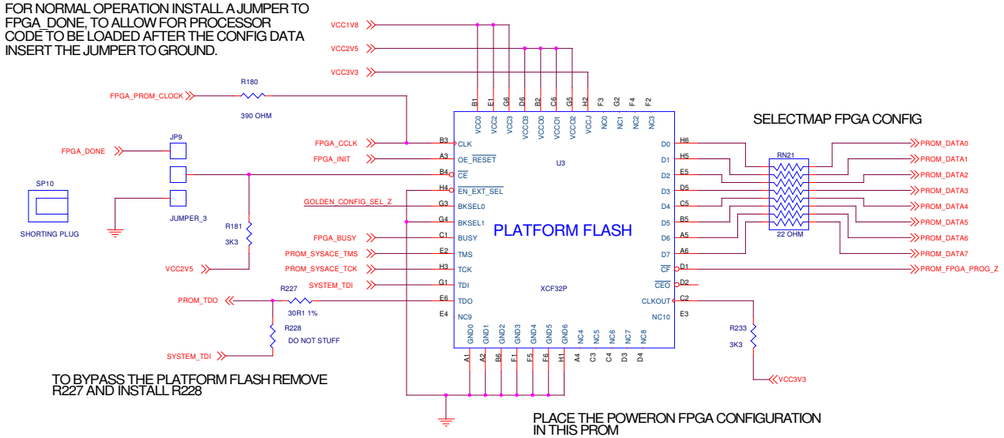




Drive the CF pin on the PROM LOW during reset to resample the version pins.

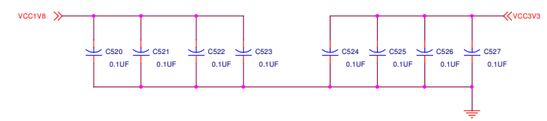


FOR NORMAL OPERATION INSTALL A JUMPER TO FPGA_DONE, TO ALLOW FOR PROCESSOR CODE TO BE LOADED AFTER THE CONFIG DATA INSERT THE JUMPER TO GROUND.

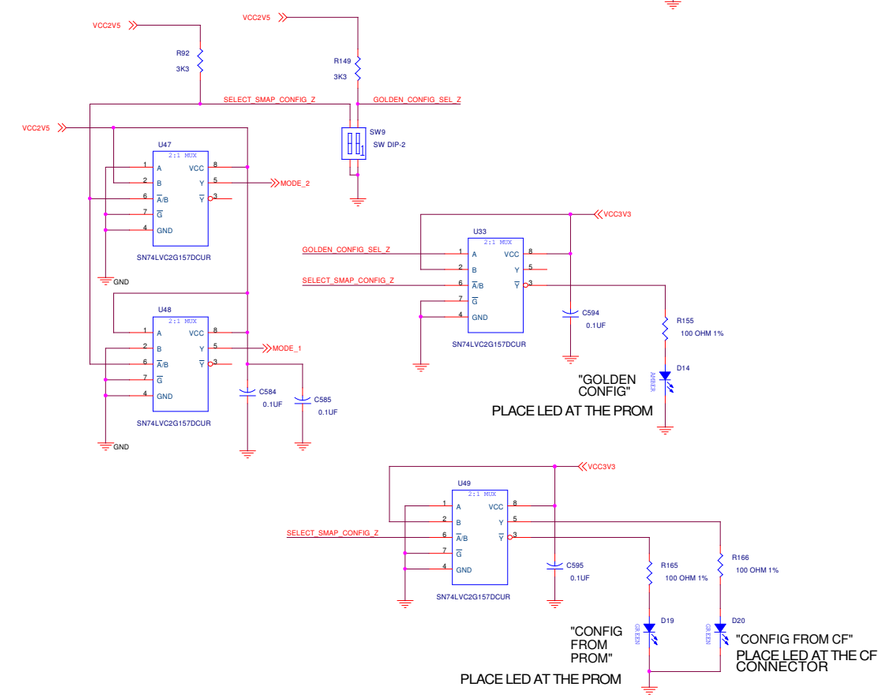


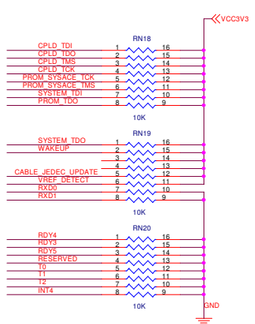
TO BYPASS THE PLATFORM FLASH REMOVE R227 AND INSTALL R228

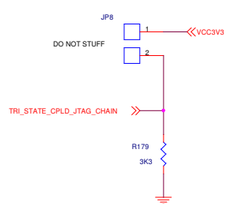
PLACE THE POWERON FPGA CONFIGURATION IN THIS PROM



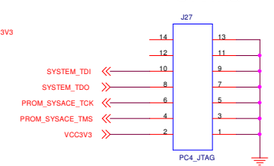
THE PLATFORM USB CABLE DETAILS HAVE BEEN REMOVED FROM THIS SCHEMATIC BECAUSE IT IS XILINX CONFIDENTIAL







PC4 JTAG



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Title: **USB CABLE EMULATION & PLATFORM FLASH**

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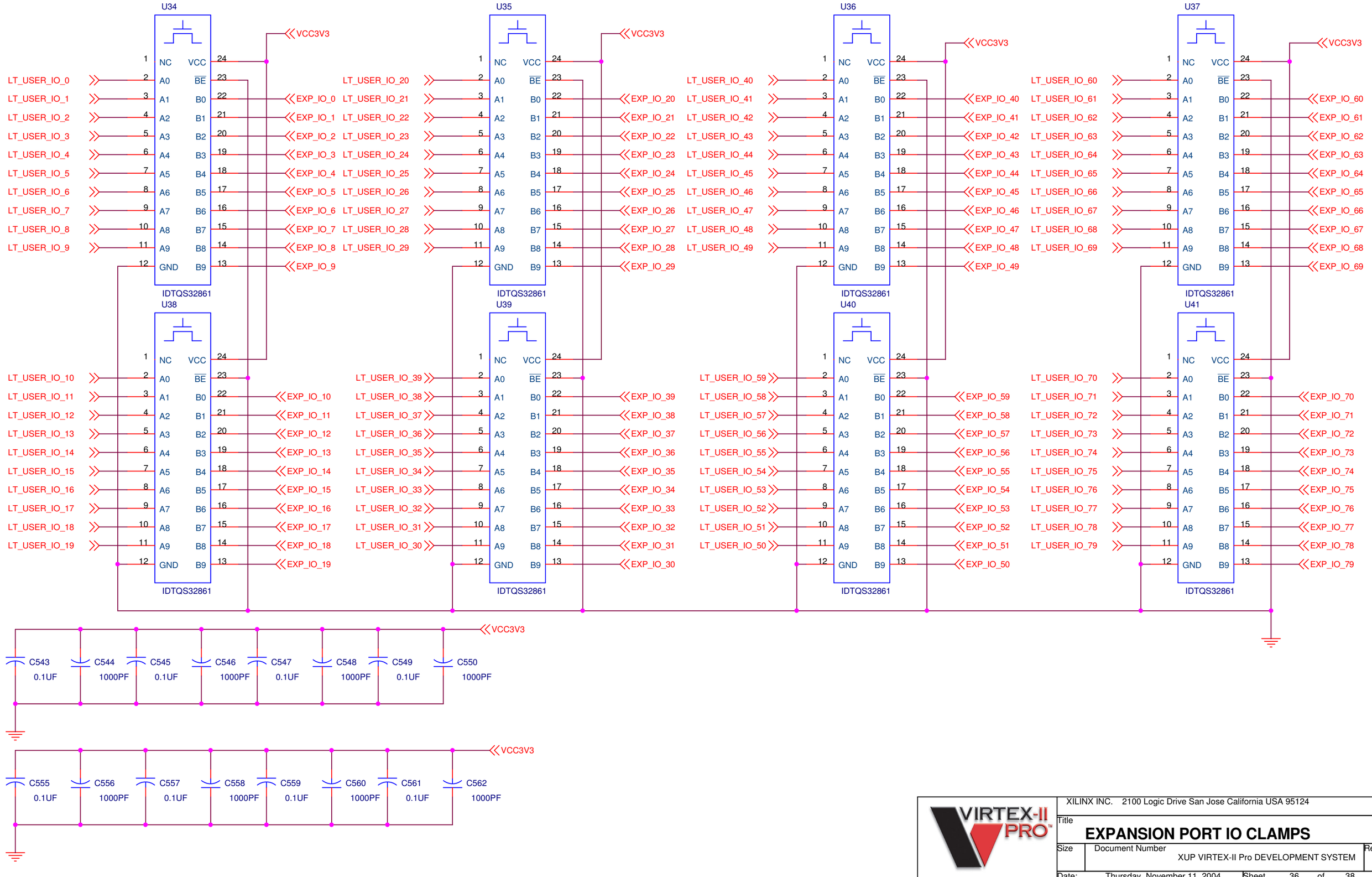

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Title

EXPANSION PORT IO CLAMPS

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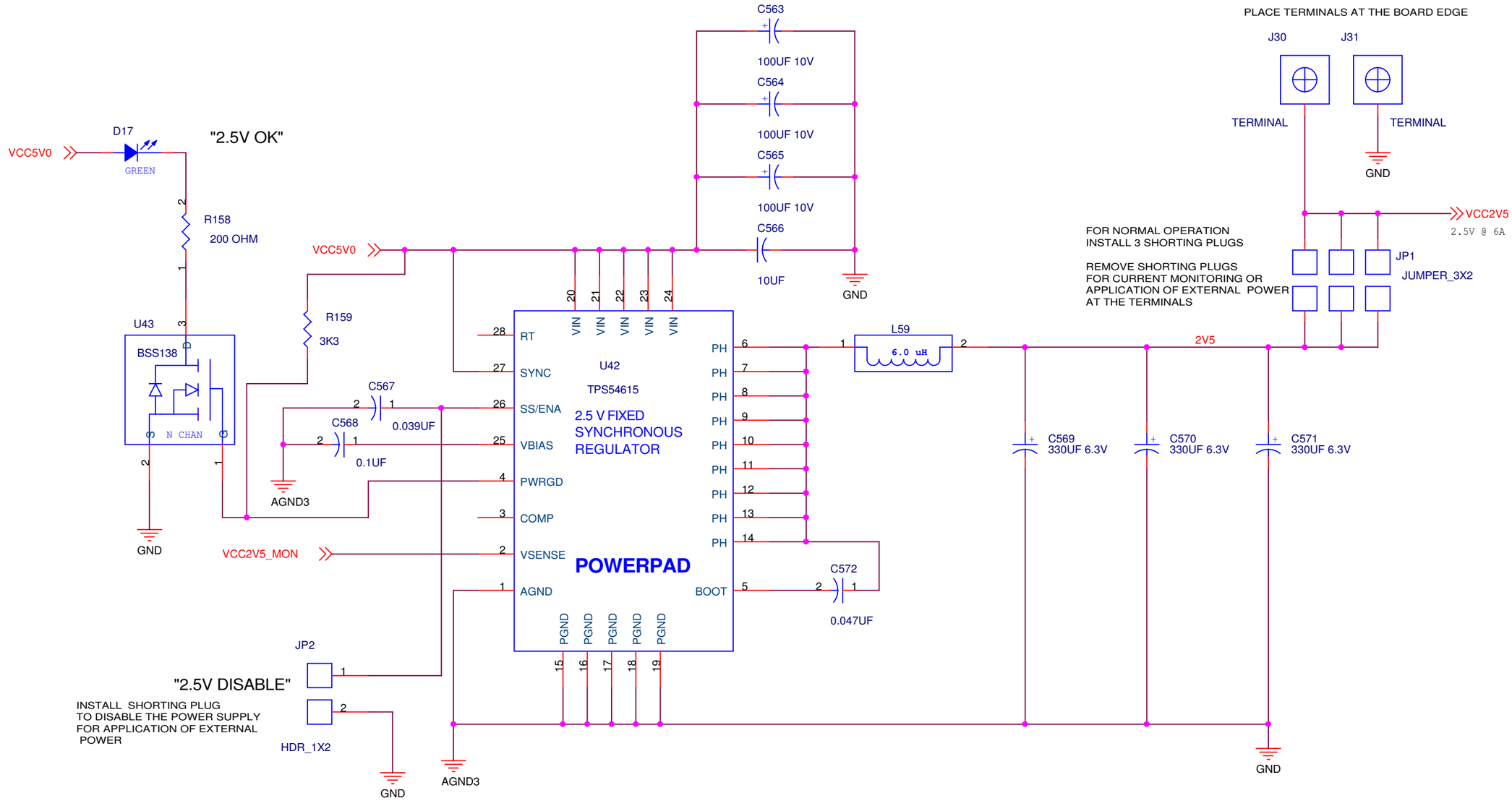
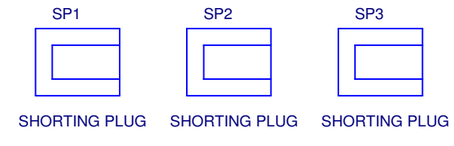


THE POWERPAD IS TIED TO AGND
FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET
CONNECT AGND3 TO GND AT PIN 1
PROVIDE A COPPER HEATSINK OF AT LEASE 2 SQ
INCHES ON TOP AND BOTTOM LAYERS



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Title
VCC2V5

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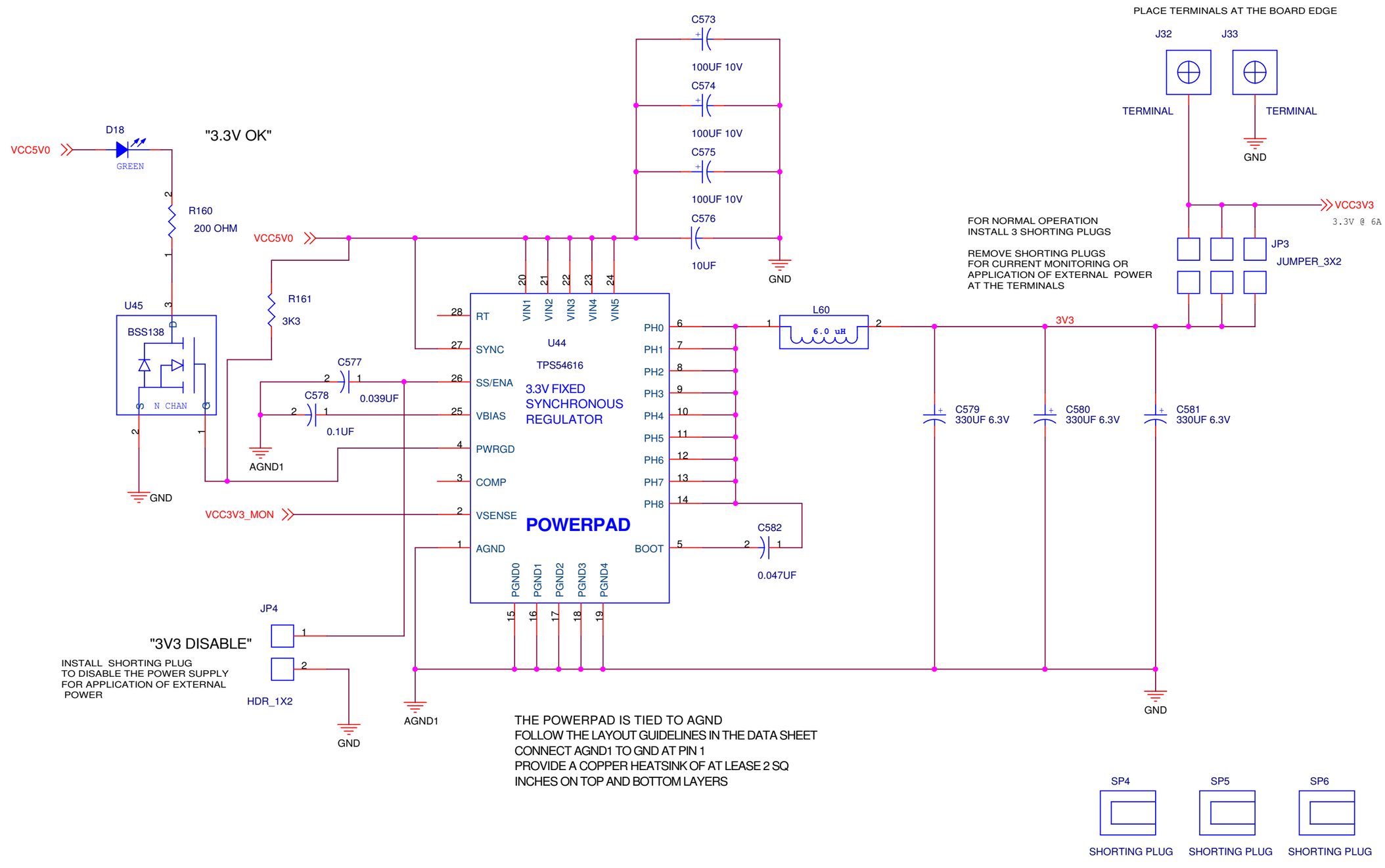

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Title: **VCC3V3**

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