THE VTT IS SPLIT INTO TWO ISLANDS EACH WITH A TERMINATION GENERATOR. THE SPLIT IS REQUIRED TO SUPPORT A CONTINUOUS CASE OF THE SDRAM BUSS CONSTANTLY DRIVEN HIGH OR LOW.

PLACE TERMINATION RESISTORS AND CAPACITORS AFTER THE DIMM SOCKET

CONNECT VSENSE TO THE MIDDLE OF THE VTT ISLAND

PLACE THE VTT GENERATOR ADJACENT TO THE VTT ISLAND

PLACE THE VTT GENERATOR ADJACENT TO THE VTT ISLAND

PLACE AT EACH END OF THE VTT ISLAND

PLACE AT EACH END OF THE VTT ISLAND
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion (if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.
PLACE DCI RESISTORS ON TOP SIDE

SDRAM_CLOCK_FEEDBACK_LOOP

R78 49R9 1%

R79

VCC2V5

SDRAM_CLOCK_FEEDBACK_LOOP

BANK 0

CENTER

CORNER
PLACE DCI RESISTORS ON TOP SIDE
PLACE DCI RESISTORS ON TOP SIDE
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion (if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

"DONE"

PLACE LED AT THE RELOAD/RESET SWITCH
DISTRIBUTE CAPS EVENLY ON ALL BANKS
DISTRIBUTE CAPS EVENLY ON ALL BANKS
THE POWERPAD IS TIED TO AGND FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET CONNECT AGND2 TO GND AT PIN 1 PROVIDE A COPPER HEATSINK OF AT LEAST 2 SQ INCHES ON TOP AND BOTTOM LAYERS

PLACE TERMINALS AT THE BOARD EDGE FOR NORMAL OPERATION INSTALL 3 SHORTING PLUGS FOR CURRENT MONITORING OR APPLICATION OF EXTERNAL POWER AT THE TERMINALS

"1.5V OK"

INSTALL SHORTING PLUG TO DISABLE THE POWER SUPPLY FOR APPLICATION OF EXTERNAL POWER AT THE TERMINALS

"1.5V DISABLE"
Distribute caps evenly on all banks
SELECT THE TDO FROM THE HIGH SPEED EXPANSION BOARD IF PRESENT.

The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

CONVERT THE 3.3V CLOCK SIGNALS ON THE EXPANSION BOARD TO THE 2.5V SIGNALS ON THE FPGA CLOCK INPUT.
### SDRAM NET LENGTH MATCHING

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<td>Clock to Clock</td>
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<tr>
<td>SDRAM_CLOCK_FEEDBACK_LOOP</td>
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</tbody>
</table>

### Notes:
- SDRAM_DQS0 - 25 mils
- SDRAM_DQS0 + 25 mils
- SDRAM_DQS1 - 25 mils
- SDRAM_DQS1 + 25 mils
- SDRAM_DQS2 - 25 mils
- SDRAM_DQS2 + 25 mils
- SDRAM_DQS3 - 25 mils
- SDRAM_DQS3 + 25 mils
- SDRAM_DQS4 - 25 mils
- SDRAM_DQS4 + 25 mils
- SDRAM_DQS5 - 25 mils
- SDRAM_DQS5 + 25 mils
- SDRAM_DQS6 - 25 mils
- SDRAM_DQS6 + 25 mils
- SDRAM_DQS7 - 25 mils
- SDRAM_DQS7 + 25 mils
- SDRAM_DQS8 - 25 mils
- SDRAM_DQS8 + 25 mils

### Differential Net Lengths:
- MGT_CLK_N to MGT_CLK_P
- MGT_RXN to MGT_TXP
- SATA_PR0_TXN to SATA_PR1_TXP
- SATA_PR0_RXN to SATA_PR1_RXP
- SATA_PR0_RXN to SATA_PR1_RXP
- SATA_PORT0_TXN to SATA_PORT0_TXP
- SATA_PORT1_TXN to SATA_PORT1_TXP
- SATA_PORT2_TXN to SATA_PORT2_TXP

### Notes:
- ROUTE AS 100 OHM DIFFERENTIAL
- TRACER WIDTH 8 mils
- TRACER WIDTH 5 mils
RESET/RELOAD

100 uSEC PULSE ON PROCESSOR_RESET_Z WHEN SW1 IS PRESSED FOR LESS THAN 2 SEC.

200 mSEC PULSE ON RESET_Z ON POWER UP OR WHEN SW1 IS PRESSED FOR MORE THAN 2 SEC.

PLACE LED AT THE RELOAD/RESET SWITCH

"RELOAD PS ERROR"

PLACE TERMINALS AT THE BOARD EDGE

PLACE SW1 BESIDE SW8 THE CONFIG SELECT SWITCH

"RESET/RELOAD"
ALL TX/RX PAIRS TO BE MATCHED IN LENGTH
AND ROUTED AS 100 OHM DIFFERENTIAL PAIRS

THE BOTTOM SIDE MGTS ARE UNUSED
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion (if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion (if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

Drive the CF pin on the PROM LOW during reset to resample the version pins.

For normal operation install a jumper to FPGA.Done. To allow for processor code to be loaded after the config data, insert the jumper to ground.

To bypass the platform flash remove R227 and install R228.

The platform USB cable details have been removed from this schematic because it is Xilinx confidential.
THE POWERPAD IS TIED TO AGND
FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET
CONNECT AGND3 TO GND AT PIN 1
PROVIDE A COPPER HEATSINK OF AT LEAST 2 SQ INCHES ON TOP AND BOTTOM LAYERS

"2.5V OK"

"2.5V DISABLE"

INSTALL SHORTING PLUGS TO DISABLE THE POWER SUPPLY FOR APPLICATION OF EXTERNAL POWER

PLACE TERMINALS AT THE BOARD EDGE
"3.3V OK"

THE POWERPAD IS TIED TO AGND
FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET
CONNECT AGND TO GND AT PIN 1
PROVIDE A COPPER HEATSINK OF AT LEAST 2 SQ INCHES ON TOP AND BOTTOM LAYERS

"3V3 DISABLE"
INSTALL SHORING PLUG TO DISABLE THE POWER SUPPLY FOR APPLICATION OF EXTERNAL POWER

PLACE TERMINALS AT THE BOARD EDGE

FOR NORMAL OPERATION
INSTALL 3 SHORING PLUGS
FOR CURRENT MONITORING OR APPLICATION OF EXTERNAL POWER AT THE TERMINALS

Xilinx Inc. 2100 Logic Drive San Jose California USA 95124