How to Live with Uncertainties: Exploiting the Performance Benefits of Self-Timed Logic In Synchronous Design

G. Paci, Giacomo.Paci@unibo.it, IMEC and DEIS, U. of Bologna, Italy; A. Nackaerts, Axel.Nackaerts@imec.be, IMEC, Belgium; F.Catthoor, Francky.Catthoor@imec.be, IMEC, Belgium; L.Benini, Luca.Benini@unibo.it, DEIS, U. of Bologna, Italy; P.Marchal, Pol.Marchal@imec.be, IMEC, Belgium

ABSTRACT

Ultra low power digital systems require the highest possible energy efficiency of logic, which can only be achieved by operating in moderate inversion. Unfortunately, when operating near the threshold voltage, transistors become highly sensitive to process variations, thereby increasing leakage currents and complicating timing closure. Rather than pursuing a worst-case design approach for dealing with these uncertainties, we present a hybrid self-timed/synchronous approach. It will be demonstrated on the VEX VLIW core designed for ultra-low-power operations. Experimental results of our approach demonstrate performance benefits up to 2x and significant energy savings at low throughput rates.

1. INTRODUCTION

Ultra low power (ULP) digital systems require the highest achievable computational performance (1-10MOPS) while consuming at most 1mW on average. The highest energy efficiency is achieved by operating in moderate inversion. Unfortunately, at these low operating voltages (near the threshold voltage), transistor switching speed and leakage power are extremely sensitive to process variations, thereby complicating timing closure of synchronous designs. Design margins at all levels of abstraction increase rapidly, causing a delay and power penalties. In this work we compare two alternative solutions for dealing with these extreme variations: the classic synchronous design based on corner point analysis and self-timed logic based on dual rail logic. Self-timed logic remains functionally correct under delay variations. Therefore, no additional design margins are needed to cope with process variations. However, the dual rail logic has high area and power overhead and requires dedicated logic libraries. Hence we propose an alternative technique to convert synchronous design into self-timed one. Rather than replacing the clock network with handshake protocol, we retain the clock and apply clock-gating until logic has completed. The completion of logic is detected using dual rail logic. To limit circuit overhead this logic is inserted only in the most critical parts/stages of the design. Experimental results on the VEX VLIW core will be presented to quantify this hybrid approach. They indicate a significant performance benefits (up to 2x) removing the pessimism of worst-case design.

2. A HYBRID SELF-TIMED/SYNCHRONOUS APPROACH DEMONSTRATED ON THE VEX VLIW

The VEX VLIW [15] consists of 4 pipeline stages (fetch, decode, execute and write back). The VLIW has been synthesized for energy with a 1.2V library, and targets a frequency of 132 MHz. Initially, its critical path (7.53ns) runs through the ALU (EX-stage), containing a 64-bit ripple adder (ALU-delay=6ns, bypass=0.84ns, others=0.68ns). To improve the average throughput of the system, we replace the ALU with self-timed logic. Other parts of the system are kept synchronous. A clock-gating mechanism is added to stall the clock as long as completion signal of the ALU is not set. In this way, the system can be operated at a higher clock frequency than the one of the synchronous ALU. In particular, the maximum clock frequency is now determined by the longest path in the remaining synchronous parts of the system, in case the decode stage which has a delay of 3.75ns. Hence, the system can be over-clocked by a factor two. As at the double frequency only very few operations of the self-timed ALU take more than one cycle, the hybrid synchronous/asynchronous design increases the throughput by a factor 1.992.

Figure 1 Better throughput/energy consumption for a partly asynchronous design of the VEX VLIW.

In Figure 1, the energy implications of this proposed system are shown. At higher voltages, the asynchronous execute stage is 1.56 times more energy-hungry compared to synchronous one. However, the energy penalty per operation for the entire system is only 21%. At lower voltages, asynchronous circuits become more efficient compared to synchronous ones. There replacing the execute stage makes the design both more energy efficient and faster.

3. CONCLUSIONS

We partially introduce a self-timed logic in an existing synchronous system by a clock-gating based solution. We have demonstrated this approach on a VLIW core. The results indicate that precise performance/energy benefits strongly depend on the specific logic architecture, but removing the pessimism inherent to worst-case design in all cases improves the throughput (up to 2x) and results in more energy-efficient designs at low operating supplies.