Statistical Variability Analysis of a Mutual Exclusion Element for Strained Silicon Processes

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Abstract
As device dimensions become smaller the impact of IC process variations on circuit properties becomes more apparent. Furthermore as superior circuit performance is sought, new technologies or circuit architectures are required. A potential candidate is strained silicon (s-Si) due to its high current drive capability attained through band gap engineering. This paper describes the investigation carried out to find the effect of process and operating condition variations on the time offset (t_{off}) and metastability resolution time (t_{m}) of a Mutual Exclusion Element (MUTEX) realized in s-Si technology. Comparison with similar devices with different strain conditions is also undertaken. The impact of process variability and variation of widths on t_{off} and t_{m} of the MUTEX are investigated using Design of Experiments (DOE) and Response Surface Methodology (RSM).

1. Introduction
The art of scaling has reached an impasse in semiconductor manufacturing regarding ITRS predictions [1]. There are some critical issues associated with scaling for example short channel effects. Low-power is identified as the most critical parameter for future circuit applications. There are several techniques proposed by circuit designers to tackle the problem associated with power consumption. Together with the circuit techniques to tackle the hurdles of future circuit design criteria, another path that could be adopted is to use materials having high carrier mobility instead of conventional Si and trading off their speed for power through supply voltage scaling. In the recent years industry has been considering the potential of band engineered s-Si devices in comparison to Si devices due to its compatibility with the existing Si process technology. Besides these electrical effects and their feasible solutions, variability is becoming a menace in the urge of scaling down to deep submicron (DSM) chip dimensions. The present work is the first of its kind which explores the process variability analysis and possibility of performance enhancement of MUTEX using s-Si devices. The choice of MUTEX is obvious as it is the basic building block of many asynchronous circuit blocks for example synchronizer, analog to digital converters, arbiters etc. and novel techniques like time amplifier [2].

Fig. 1 The family of circuit and novel technique which incorporate MUTEX as the basic building block.

The ITRS device parameters have been used for the device and circuit simulations [1]. To study the impact of variability in the manufacturing of transistors on t_{off} and t_{m} of MUTEX the statistical method of DOE/RSIM is applied due to its computational efficiency over Monte Carlo technique [3]. The entire work is performed by developing Si and s-Si technology library by simulations using TSUPREM4 (process simulator), MEDICI (device simulator), AURORA (parameter extraction program), and PSPICE (circuit simulator) subjected to different operating conditions, device dimensions and band gap engineered devices [4]. MINITAB is used for the statistical DOE analysis. State of the art 65nm technology node designed for high performance (HP) is taken into consideration [1]. Our work shows that under the scaled supply voltage conditions and scaled dimensions, the s-Si MUTEX performs better compared to the similar Si based MUTEX. The variability analysis method using DOE/RSIM statistical analysis for studying process variability and statistical analysis of t_{off} and t_{m} of MUTEX are performed in section 3. The subsequent conclusions are outlined in section 3.

2. Variability analysis flow
The flow chart of the analysis to study the variability of process parameters is shown in Figure 2. State of the art 65nm technology is chosen as the technology node of choice as its variability is seen to be larger in comparison to similar 300nm technology node [5]. 19 parameters are identified from the 65nm process as the important parameters at different process steps. The parameters are all varied over a range of 10% from its nominal value. However, the temperatures are varied as ±5°C from the nominal. Due to the fact that the modeling of 19 parameters using RSM needs 524288 simulations (2^{n+2n+1}, where n is the number of parameters) [21] and hence computationally inefficient like Monte Carlo, a statistical screening technique (PB screening) [20, 21] is used to identify the significant parameters.
Simulations of MUTEX are performed using 65nm bi-axial s-Si and Si transistors developed using MEDICI and TSUPREM4 based on ITRS specifications. Channel of each transistors are subjected to strain which ranges from 0% (conventional Si) to 0.99% (s-Si). The 0.99% strain is equivalent to 25% Ge in the wafer (bi-axial strain). The s-Si inherently has higher transconductance and lower threshold voltage compared to that of Si due to the presence of strain and smaller band gap [4]. However, it is not expected to continue the same trend with the increase in the amount of strain. This is due to the fact that the enhancement of the performance in the transistors is found to degrade when the amount of strain increase beyond 0.99% [4]. Hence the analysis presented here is limited to 0.99% strain.

The ratio of widths of p-MOS to n-MOS devices in MUTEX is considered as reported in [2]. However, it should be noted that since the enhancement of mobility of holes and electrons due to different amount of strain are different and hence there is an added flexibility for the designers in choosing the area of the devices. The simulations are performed at supply voltages ranging from 0.9V to 1.3V for the transistors under different process conditions. The supply voltage is limited to the above range as is specified by ITRS for the HP devices. Simulations are done for MUTEX realized with s-Si transistors with varying strain in the channel (0.99%, 0.495 and 0%). The offset time of MUTEX is calculated.

toff is giving a large range of variation for Si when Nsub is changing 10% from the nominal which is undesirable. When strain in the channel of transistors is increasing, the variation of toff with Nsub is not high as compared to Si which is shown in Figure 3. Figure 4 shows the variation of toff with Nsub and tox. toff is decreasing with increasing Nsub and when tox is reduced. toff is seen to be less when Nsub is large and tox is small. Figure 5 show that t_m is increasing with tox. For different amount of strain (Si and s-Si), when strain increases t_m is not linear which is due to the interaction between the two process parameters; strain and tox.

3. Conclusion

We have investigated the DOE/RSM methods for studying the impact of process variability on metastability resolution time (t_m) and offset time (toff) of MUTEX. Plackett-Burman screening is used to screen the insignificant parameters and, models based on significant parameters are developed using RSM which models the interaction effects also. Interaction of process parameters in three dimensional spaces has been studied. The variation of strain in the channel is found to be the most significant process parameter.

References