SiGe HMOSFET DIFFERENTIAL PAIR

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ABSTRACT

A SiGe HMOSFET can be engineered to provide enhanced linearity in its output current-voltage characteristics. The additional linearity can be exploited in the design of more linear analogue circuits like the differential pair presented here. From the TCAD data of such a structure, the BSIM3v3 model of the transistor was extracted and simulation results were obtained for the performance of a differential pair. At the specified power of 1.25mW the input range of the SiGe differential pair at which the percent nonlinearity is bellow 1%, is roughly twice of its Si counterpart. Additionally the SiGe circuit is more power efficient since an increase of the power consumption from 1mW to 1.25mW accounts for an improvement of about 40% in its input range, as compared to only 10% for Si.

1. INTRODUCTION

The introduction of SiGe layers is not a new development in the semiconductor industry. It has been successfully used over the past years to built high performance heterojunction bipolar transistors (HBT) [1]. The use of a heterojunction enhances the electrical properties of the bipolar transistor, making bandgap engineering a valuable tool. This method has been recently introduced to MOSFETs by using SiGe again. The recent research on SiGe HMOSFETs (Heterojunction MOSFETs) [2],[3] is strongly motivated by the anticipated compatibility with the existing Si CMOS fabrication technology. SiGe HMOSFETs are manufactured using the same fabrication steps of a commercially available Si CMOS technology. Therefore the realization of these transistors from existing Si CMOS production lines is feasible, although minor refinements will be required. At the same time, SiGe HMOSFETs can operate at a higher frequency when compared with their CMOS counterparts with the addition of a higher transconductance [4-6]. The most attractive benefit of using SiGe transistors however, is the fact that their structure can be engineered to provide a specific pattern in the output characteristics (namely g_m and I_{DS}-V_{GS}), by carefully selecting the various structure parameters (different layers, their composition, doping and thickness) of the device [6].

The SiGe HMOSFET contains a buried channel within a high mobility strained layer of material, which is usually Si, but can also be a SiGe layer with different composition with respect to the substrate, or even pure Ge [2]. The channel is separated from the gate oxide by a SiGe cap layer. Inside the strained layer (channel), a two-dimensional electron gas is formed with an enhanced mobility compared to the conventional Si inversion MOSFETs.

By carefully selecting the layers of the device a more linear SiGe transistor can be built when compared to a conventional Si MOSFET. The transistor is first simulated with the TCAD simulator MEDICI [7] and a device model using the BSIM3v3 parameters [8] is extracted. Simulations were performed with SPICE under the Cadence environment, where a comparison was made with a conventional and commercially available Si MOSFET technology (available through the MOSIS service [9]) via its BSIM3v3 transistor model.

In this work the advantage of using a SiGe HMOSFET differential pair is presented, focusing on the increased linearity that the SiGe device can deliver to the differential pair. This is reflected at the increased input voltage range and also at the power handling capability of the circuit.

2. SiGe HMOSFET

2.1 Structure Design

One way to build SiGe HMOSFETs is the growth of a thin and therefore strained Si layer on top of a SiGe substrate [2]. However, compatibility with existing Si technology, requires that a Si substrate be used with the rest of the layers grown on top of it. As a result the SiGe layer has to be grown thick onto Si, in order to be relaxed. This is called the 'virtual substrate' technique [2]. A large number of structures arise when varying the thickness of the various layers, the germanium content and the doping. The motivation for the structure of this work was to increase the linearity of the transistor and study the impact at circuit level. One such structure was found to be the one presented in figure 1.

The germanium concentration is 0.1 for both the virtual substrate material and the 2 nm thick SiGe cap layer, which is required.

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The virtual substrate layer is p type doped at $2.1 \times 10^{17} cm^{-3}$ while the SiGe cap layer is undoped to improve mobility. A 7 nm thick gate oxide is included. The low Ge mole fraction allows easier transfer of electrons from the buried Si channel to the surface SiGe channel, at higher gate biases, which improves device linearity at the expense of some transconductance.

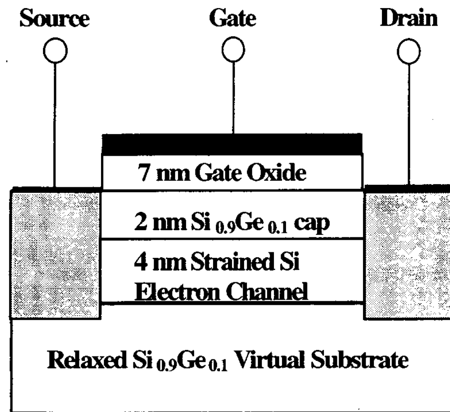

Figure 1. Layer structure of SiGe HMOSFET

At lower gate biases the dominant channel is restricted within the strained Si layer. A two-dimensional electron gas with enhanced mobility is formed, which is responsible for the high transconductance of the device. At higher gate voltages the lower mobility SiGe cap layer is also inverted, contributing to the transistor effect. This is expected to increase the linearity of the device.

2.2 Model extraction and verification

The SiGe HMOSFET fabrication technology, although very promising, is not yet mature enough to provide reliable and fully characterized devices and models. Thus, the models used so far, mainly rely on device simulators, which produce the output characteristics of a given structure. The device shown in figure 1 was simulated using the two-dimensional technology computer aided design (TCAD) tool MEDICI [7]. The software has been previously calibrated against experimental data [4],[5]. Using I_{DS}-V_{GS} and g_m-V_{GS} data generated in this way, BSIM3v3 [8] compact model parameters for the SiGe HMOSFET were extracted, which fitted the behavior described by MEDICI. This BSIM3v3 model was then used throughout all the simulations.

The choice for a BSIM3v3 model was made because of its proven capability of successfully describing modern Si MOSFETS. This is done by the use of several fitting parameters that describe the physics of a MOSFET. However, a SiGe HMOSFET is a more complex device, due to its two-dimensional electron gas. So, the model was carefully used without its scaling feature, and for every different aspect ratio transistor that was used, a separate model was extracted.

The verification of the quality of the fit was done via SPICE, by comparing the characteristic I_{DS}-V_{DS} curves over the operating V_{GS} range (0 – 3 V). For comparison, a conventional Si device was used, represented by its BSIM3v3 model from a commercially available and scalable process (through the MOSIS service [9]). Both SiGe and Si transistors have a gate-length of 350 nm.

2.3 Transistor Transconductance

The simulated g_m versus V_{GS} behavior at saturation is shown in Fig. 2, for both types of devices. It is clear that the transconductance of the Si MOSFET increases monotonically with V_{GS} over the entire range of realistic overdrive voltages ($V_{GS}(DC)$-V_T, V_T is the threshold voltage) used in circuit design. On the other hand, the transconductance of the SiGe device, after a steep increase, reaches a maximum value, which is maintained for higher gate voltages. This flat transconductance region reflects a linear I_{DS} dependence on V_{GS}, which proves to be very attractive for the design of more linear analogue circuits. Of equal importance is the fact that, for a given gate bias, the transconductance is always higher for the SiGe HMOSFET. It increases more rapidly than the Si MOSFET, and the maximum value is obtained at a relatively low gate-to-source voltage, leaving plenty of usable gate overdrive for linear output current operation.

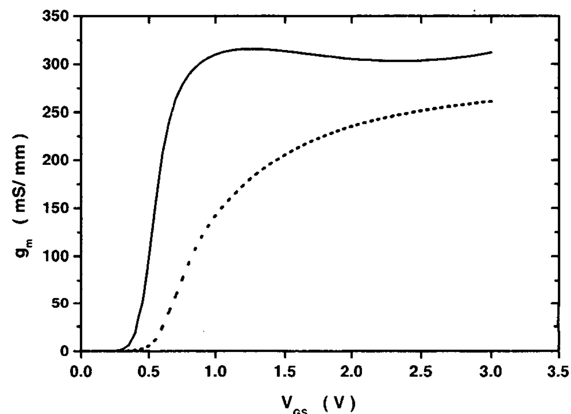

Figure 2. SiGe (solid line) against Si (dashed line) transconductance

3. DIFFERENTIAL PAIR

3.1 Circuit Description

The differential pair [10] is an essential component of most modern analogue circuits, wherever a voltage to current conversion is required. It can be used in the input stage of an amplifier and also as part of transconductors. Therefore, the idea of having a more linear differential pair is worth investigating. So, it is interesting to identify what is the impact of using a more linear device, like the SiGe HMOSFET presented in the last paragraph, to build such a basic cell like the differential pair (the effect of exploiting this linearity in the design of a single

balanced mixer has been shown in [11]). By enhancing the linearity of a circuit its dynamic range is potentially increased, assuming that the noise is not significantly affected.

The differential pair is presented in figure 3. It comprises of transistors M1 and M2. They are biased through the current source I_{ss}. A common mode DC voltage is applied to the gates of the transistors, since the power supply is not symmetrical (it ranges from V_{dd} to ground). The currents flowing through M1 and M2 are I_1 and I_2 respectively. The input is applied differentially to the two gates of the transistors, as shown in the figure.

When no signal is applied currents I_1 and I_2 are equal, namely $I_{ss}/2$, and the transistors are biased in exactly the same way (assuming same geometries). When a positive input voltage is applied to the gate of M1, the current I_1 is increased, resulting in a decrease of I_2 (since their sum should equal I_{ss}). The two branches of the circuit are loaded with the same resistance R, and the output current is assumed to be the difference between I_1 and I_2.

The differential pair performs a V to I conversion. Its response is measured by the transconductance, which is equal to :

$$g_m = \frac{d(I_1 - I_2)}{dV_{in}}$$

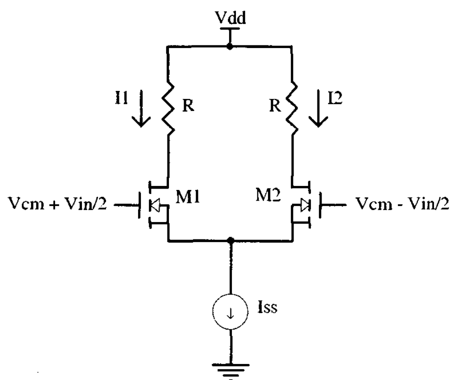

Figure 3. Differential pair

3.2 Simulation Results

The large signal performance of the differential pair is reflected at its nonlinearity. This nonlinearity is defined as the percent deviation from the maximum small signal g_m value of the circuit. At low input signal levels the differential pair is essentially a linear transconductor. As the signal level increases, a deviation from the linear behavior occurs. This effect limits the input range of the differential pair and consequently the dynamic range of the cell. This deviation is caused primarily by the nonlinearity of the device. In the case of Si MOSFET, where the well-known square law dependence between the gate source voltage and drain current is assumed, the nonlinearity can be calculated theoretically [12]. In the case of SiGe HMOSFET however, there is no closed form relationship between the input gate source voltage and the drain current, and so no straightforward theoretical calculations can be made. Despite this, figure 2 shows that a more or less constant g_m occurs over a given range of V_{GS}. The nonlinearity results for the differential pair of figure 3 are shown in figure 4. These results were obtained by using 100 Ω load resistances, a rail voltage of 2.5 V and a DC common mode voltage of 1.25V., In both Si and SiGe circuits the transistors were 0.35μm long by 1μm wide. In order for these devices to acquire the proper overdrive voltage (V_{GS}-V_T) four such parallel devices were used for each side of the Si pair and two for the SiGe pair. The solution of connecting parallel devices to form each of the transistors M1 and M2, which are depicted in figure 3, was chosen due to the scaling restrictions, which were mentioned earlier in paragraph 2.2. An I_{ss} current of 0.5 mA is drawn in both Si and SiGe circuits, bringing the DC power consumption at 1.25 mW.

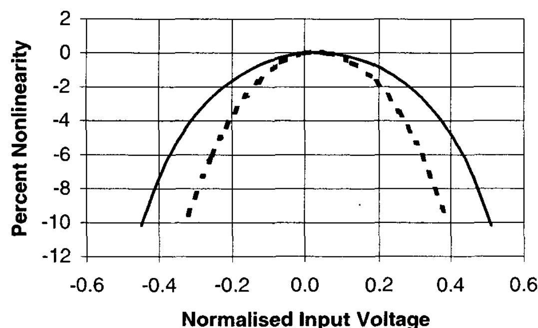

Figure 4. Percent Nonlinearity of the SiGe (solid line) and Si (dashed line) differential pairs

The horizontal axis of figure 4 is the normalised input voltage of the circuit. The normalisation has been made with respect to the DC common-mode bias, which is present at the gates of both circuits (1.25V). This choice was preferred instead of using the characteristic voltage $\sqrt{I_{ss}/K}$ (which is used in [12]), since the square law does not hold for the SiGe device. The vertical axis of the circuit represents the percent nonlinearity as a deviation from the maximum small signal transconductance of the cell. This value occurs at low input signal, ie around the normalised value of zero.

From figure 4 it can be observed that the normalised input range of the differential pair at which the output percent nonlinearity is bellow 1% is roughly twice for SiGe compared to the Si circuit. This gives the advantage to the SiGe differential pair of being able to operate with less distortion for the same input voltage than the Si one, or equivalently, the ability to accept a higher input signal for a specified distortion level. Si circuits in most cases have to be more complex to achieve this [13].

In figure 5 the effect of varying the dissipating power of the circuits, by altering the current, is presented. The vertical axis shows the normalized input range for 1% nonlinearity. By increasing the tail current of the circuit, or equivalently its power consumption, the output linearity of the circuit increases. This increase in linearity is represented as an increase in the normalised input range, depicted in figure 5. An increase of the power consumption from 1mW to 1.25mW accounts for an improvement of about 40% in the input range of the SiGe circuit, as compared to only 10% of Si. This corresponds to a far more efficient power handling capability of the SiGe circuit when compared to the Si one.

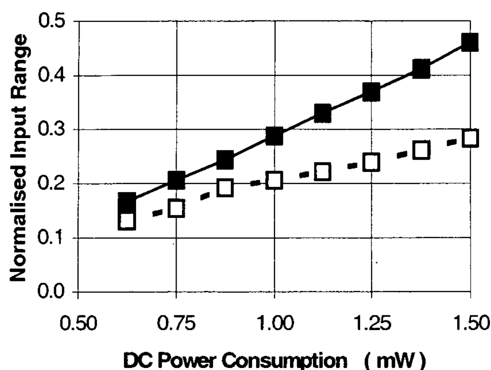

Figure 5. Normalised Input range of SiGe (solid line) and Si (dashed line) differential pair

4. SUMMARY

In this paper a properly designed SiGe HMOSFET and its circuit application is demonstrated. The purpose of this design is to produce a device that is more linear in terms of I_d-V_{GS} characteristics and consequently investigate the effect of such a design at circuit level. TCAD simulations provided the necessary data to evaluate the device, while an extracted BSIM3v3 model was used to simulate a simple differential pair circuit. In all simulations, the Si and SiGe circuits were treated in the same way to highlight how the enhanced linearity of a single device can be exploited in such a basic cell like the differential pair.

The SiGe circuit can give almost two times higher input range for a specified 1% output nonlinearity. This identifies the SiGe HMOSFET, and consequently the SiGe circuits, as a serious contestant in highly linear applications, a performance for which the Si based circuits have to be more complex to manage. Basic SiGe building blocks, like the differential pair, due to their intrinsic linearity, can handle power much more efficiently than Si does. An increase of about 0.25mW in the DC power consumption is translated into a 40% increase in the normalized input range for the SiGe circuit, while for the Si one the enhancement is only 10%. This power handling performance makes the SiGe differential pair a preferred choice for high linearity – low power consumption applications.

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5. REFERENCES

[1] Luy, J.-F., Russer, P., *Silicon-Based Millimeter-Wave Devices*, Chapter 4, Springer –Verlag, 1994.

[2] Schaffler, F. "High-mobility Si and Ge structures", *Semiconductor Science Technology*, 1997, Vol 12, pp 1515-1549.

[3] Paul, D.J. "Silicon germanium heterostructures in electronics: the present and the future", *Thin Solid Films*, 1998, Vol 321, pp 172-180.

[4] O'Neill, A. G., and Antoniadis, D. A. "Deep submicron CMOS Based on Silicon Germanium Technology", *IEEE Trans. Electron Devices*, June 1996, Vol. 43, pp. 911-918.

[5] O'Neill, A. G., and Antoniadis, D. A. "Investigation of Si/SiGe-Based FET Geometries for High Frequency Performance by Computer Simulation ", *IEEE Trans. Electron Devices*, Jan. 1997, Vol. 44, pp. 80-88.

[6] Halkias, G., and Vegiri, A.: "Device Parameter Optimization of Strained Si Channel SiGe/Si n-MODFET's using a One-Dimensional Charge Control Model", *IEEE Trans. Electron Devices*, Dec. 1998, Vol. 45, pp. 2430-2436

[7] Avant!, *Medici User Manual*, 1998.4.1.0 ed., Freemont, CA, Avanti Corporation, 1998.

[8] Cheng, Y., Chan, M., Hui, K., Jeng, M. C., Liu, Z., Huang, J., Chen, K., Chen, J., Tu, R., Ko, P. K., and Hu, C. *BSIM3v3 Manual*, University of California, Berkeley, CA 94720, 1996.

[9] *The MOSIS Service*, USC Information Sciences Institute, 4676 Admiralty Way, 7th floor, Marina del Rey, CA 90292-6695, USA.

[10] Sedra, A. S., Smith, K. S., *Microelectronics Circuits, Paragraph 6.6, Forth Edition*, Oxford University Press, 1998.

[11] Badcock, S.G., Despotopoulos, S., Michelakis, K., Papavassiliou, C., Chester., E.G., O'Neill, G. O. and Toumazou., C. "Improved Linearity using SiGe HMOSFETs", *Submitted to Electronics Letters*.

[12] Toumazou, C., Lidgey, F. J., and Haigh, D. G. *Analogue IC Design: the Current-Mode Approach*, Chapter 5, Peter Peregrinus Ltd. on behalf of IEE, 1993.

[13] Johns, D.A, Martin, K., *Analog Integrated Circuit Design*, Chapter 15, John Wiley & Sons, 1997.