SiGe HMODFET "KAIST" Micropower Model and Amplifier Realization

Antonio Vilches, Kristel Fobelets, Kostis Michelakis, Solon Despotopoulos, Christos Papavassiliou, Thomas Hackbarth, and Ulf König

***Abstract*—The recently published small-signal KAIST model is used successfully to fit the measured RF characteristics of a novel SiGe n-HMODFET device operating at micropower levels and extracted small-signal model parameters for this device under micropower operation are presented here for the first time. This model is then used to predict the performance of a simple micropower amplifier (sub 300-μW total power consumption), realized in SiGe technology, and a comparison of modeled versus measured data is included.**

***Index Terms*—Micropower, modeling, MODFET, SiGe.**

I. Introduction

WORK on buried channel SiGe/Si hetero-junction FET devices began in the early 1980s with a view to exploiting the higher mobilities offered by the strained channel in order to improve the speed of pMOS devices [1]. The work was then expanded to n-type HMODFET devices by fabricating the active n-type layers on relaxed p-type SiGe buffer layers, originally in [2] and [3], and more recently in [4]–[6]. It was soon realized that the increased mobility in buried channel devices, due to a lower subthreshold slope at low to high V_T, offered the prospect of reducing power supply levels for RF operation to what are here broadly termed micropower levels (sub 1-mW total power consumption) [7]. Such low-power, RF capable devices would clearly improve battery life and reduce overall heat dissipation in sensitive, long-term portable RF and biomedical applications.

Although a range of device fabrication techniques are under exploration including the use of a grown or sputtered gate oxide to reduce gate currents [8], [9] and fabrication on insulating substrates to reduce parasitic effects and so improve RF performance [10], [11], SiGe HMODFET device modeling for RF micropower applications is still at a very early stage and there is currently no published small-signal modeling data for SiGe virtual substrate (VS) n-HMODFET devices operating with a total power consumption of sub 300 μW. In this paper, we report on the first-time use of the recently published KAIST small-signal model and simple, linear regression based parameter extraction process [12] for micropower small-signal RF modeling of n-HMODFET devices, which we find to be more suitable than the related approaches previously discussed in [14]–[20].

The device structure and fabrication is outlined in Section II-A, the extraction method used is briefly discussed in Section II-B, extracted small-signal parameters and modeled versus measured device comparison are presented in Section III-A, simulated versus realized micropower amplifier characteristics are given in Section III-B, and we conclude in Section IV.

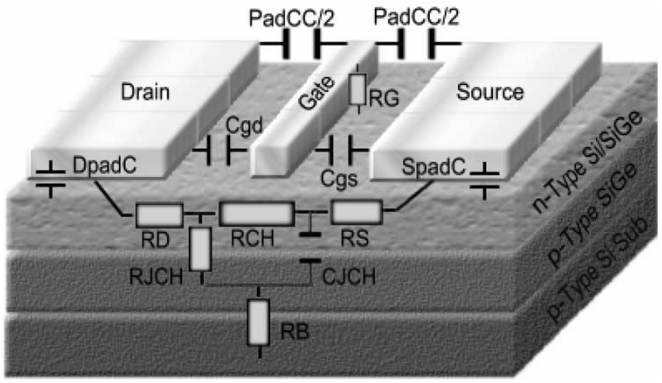

Fig. 1. A n-HMODFET device physical structure and equivalent circuit diagram.

3.5 nm Si cap
6 nm SiGe cap 40%
5 nm n^+-SiGe 40% : Sb supply
3.5 nm SiGe 40% spacer
9 nm Si channel
4 nm SiGe 40% spacer
5 nm n-SiGe 40% :Sb supply
150 nm SiGe 40%
LEPECVD 40% 5 μm
Silicon substrate: p- > **1000** Ωcm Total MBE Epi: 186 nm

Fig. 2. Device stack layer details.

II. Method

A. Device Structure and Fabrication

A diagram of the device's physical layer structure overlaid with equivalent circuit small-signal circuit parameters is shown in Fig. 1; the stack layer details are given in Fig. 2, and Fig. 3 is an actual photomicrograph of the RF device under test (DUT). The transistors are "T" types, so called because they possess a single gate-pad driving a metal gate-finger split symmetrically between source and drain, as shown in Fig. 3. Devices of 0.1-μm gate length and 100-μm width were used for this investigation.

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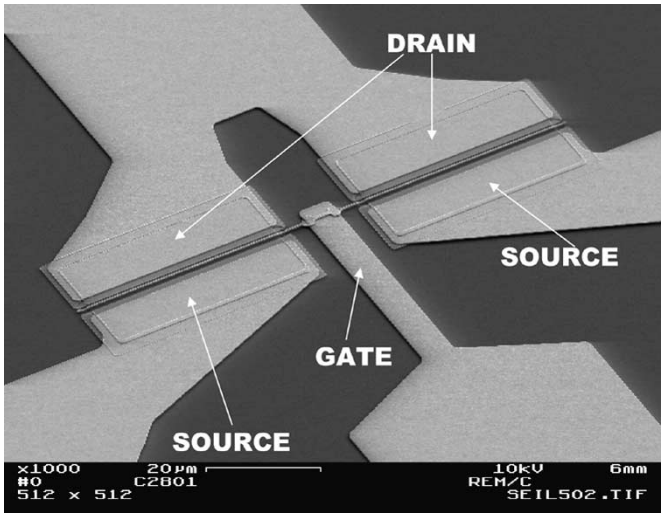

Fig. 3. Photomicrograph of "T" type HMODFET device with gate, drain, and source contacts labeled.

The n-MODFET structure was grown by molecular beam epitaxy (MBE) on a 40% (Ge) graded VS, which was prepared by low-energy plasma enhanced chemical vapor deposition (LEP-ECVD). Free electrons are supplied into the 9-nm strained Si channel by two Sb-doped layers, which are situated on either side of the quantum well. These layers are separated from the channel through the use of undoped SiGe spacer layers to reduce scattering and further enhance the channel mobility. The structure is capped with a 6-nm SiGe layer and a thinner Si layer on top to ensure the highest possible quality for the metal Schottky gate.

A standard fabrication technique for n-type SiGe MODFETs was applied, which included dry MESA etching for electrical isolation of the epitaxial active areas and deposited field oxide for electrical isolation of the implanted areas. The ohmic contacts were implanted with P and were subsequently activated by rapid thermal annealing (RTA). The ohmic metal consisted of Ti/Pt/Au and was implemented by optical lithography, e-beam evaporation, and lift-off and is also used for circuit interconnections. The Pt/Au Schottky gates were defined by e-beam lithography plus lift-off. The minimum gate length available on-wafer is 0.1 μm. A number of test devices and structures were also included for characterization, among which were Hall patterns which were characterized at 300°CK. The measured sheet resistivity of the structure was 811 $\Omega/\square$, the sheet electron density was 4.5×10^{12} cm^{-2}, and the corresponding mobility was 1700 cm^2/Vs (300°CK). Measured mean access resistance values of 3 Ω·mm for drain and source resistances (RS and RD) were provided by the DaimlerChrysler foundry. The unusually high mean value of these access resistances is expected to dramatically reduce as the technology used matures and processing technique is improved.

B. Simulation, Modeling and Parameter Extraction

A HP5783D Network Analyzer was used to probe, bias and measure the fabricated devices and the recorded two-port s-parameters were converted into Y parameter sets, using MWOFFICE CAD software [21], for use in direct extraction and modeling.

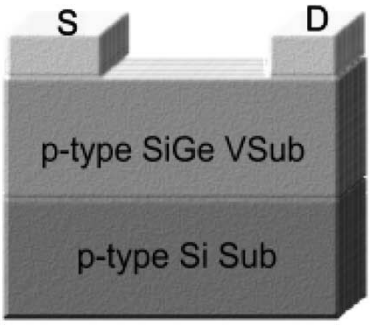

Fig. 4. Simplified diagram of the "open" structure. Source and drain metal contacts, denoted by letters "S" and "D," are separate.

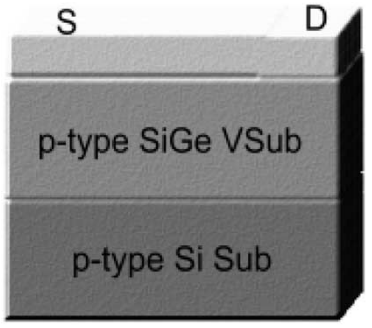

Fig. 5. Simplified diagram of the "short"' structure. Source and drain metal contacts, denoted by letters "S" and "D," are shorted together.

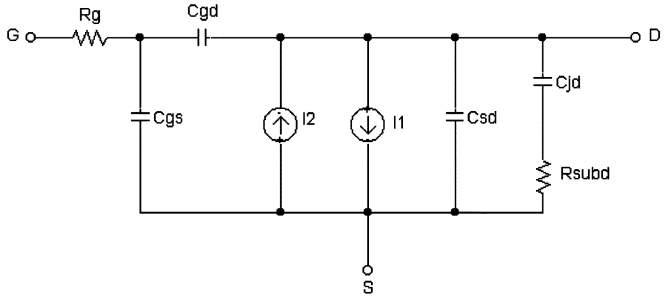

Fig. 6. KAIST small-signal equivalent circuit model of the intrinsic device.

The device was biased in the subthreshold region: $V_{\rm GS} = -0.8$ V as this is close to its threshold voltage of -0.88 V. A $V_{\rm DS}$ supply of 400 mV was used and the supply current for this setup was measured at 734 μA, giving a total supply power of 294 μW.

The intrinsic device was de-embedded using the lumped-element de-embedding technique reported in [13] with the aid of further data sets measured from "open" and "short" devices located on-wafer close to the DUT, simplified diagrams of which are shown in Figs. 4 and 5. It was not considered necessary to model inductive parasitics as an s-parameter extracted track inductance value of 714 nH/m indicates that the effect of these at the frequencies dealt with would be negligible. The extraction process for the intrinsic device parameters ($g_m, g_{\rm ds}, R_g, C_{\rm gd}, C_{\rm gs}$, and $C_{\rm dg}$) given by Kwon *et al.* in [12] was then rigorously followed in order to obtain their values for the KAIST model shown in Fig. 6. The current sources I_1 and

I_2 computed during simulation as given in (1) and (2) from [12] are

$$I_1 = g_m V_{\rm gs} \tag{1}$$

$$I_2 = (C_{\rm dg} - C_{\rm gd})\frac{dV_{\rm gs}}{dt}. \tag{2}$$

Confusion arose during the extraction of the substrate parameters when it was realized that the equation given for $Y_{\rm sub}$, [12, eq. (15)] is a function of source-drain capacitance $C_{\rm sd}$. This parameter, it was claimed, is to be obtained from (18) in [12] *after* $Y_{\rm sub}$ has been evaluated, as $C_{\rm sd}$ is a function of both $R_{\rm subd}$ and $C_{\rm jd}$, which are both, in turn, functions of $Y_{\rm sub}$. Private communication with the author on this issue confirmed that the inclusion of the term $-jwC_{\rm sd}$ in equation for $Y_{\rm sub}$ was a typographical error and that this term could be safely omitted from the calculation. It is to be noted also that the extracted value for $C_{\rm sd}$ reported in [12] is small and negative (-3.1 fF) as it is in our own extraction and this casts doubt on the validity of the use of this parameter in the model as it is suspected that $C_{\rm sd}$ and $C_{\rm jd}$ combine to give an accurate value for $C_{\rm jd}$. The remaining substrate parameters ($R_{\rm subd}, C_{\rm jd}$ and $C_{\rm sd}$) were then extracted as explained in [12] only with the $-jwC_{\rm sd}$ term omitted from the $Y_{\rm sub}$ equation and the small-signal KAIST model together with a comparison of the modeled versus measured intrinsic device admittance versus frequency is given in the results section.

The extracted model is then used to simulate a simple Class-A micropower amplifier in MWOFFICE, with an input power level of $-$ 25 dBm and a total power supply to the FET device of just 294 μW. The FET is worked into a resistive 120-Ω load, and no impedance matching is used as the circuit's bandwidth was expected to be low at the targeted micropower operation level; the circuit's input and output are terminated with standard 50-Ω ports. Plots of power gain $G_{\rm MAX}$ (3) and maximum stable gain [MSG—(6)] are used in Section III-B to illustrate and compare the gain and bandwidth of both the simulated and measured amplifier response

$$G_{\rm Max} = \frac{|S_{21}|}{|S_{12}|}(k - \sqrt{k^2 - 1}) \tag{3}$$

where

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}||S_{21}|} \tag{4}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5}$$

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|}. \tag{6}$$

III. Results

A. Device Model and Parameters

A plot of the de-embedded bonding-pad capacitances as a function of measurement frequency is shown in Fig. 7. A mean extracted value of 115 fF is shown for the drain and gate capacitances *CpadD* and *CpadG*, respectively, and a mean value of 4.8 fF is shown for the parasitic coupling capacitance between gate and drain, *PadCC*. The deviation from the expected mean values at low frequencies is due to a combination of current leakage in the pads and the inherent low frequency roll-off of the network analyzer's port couplers.

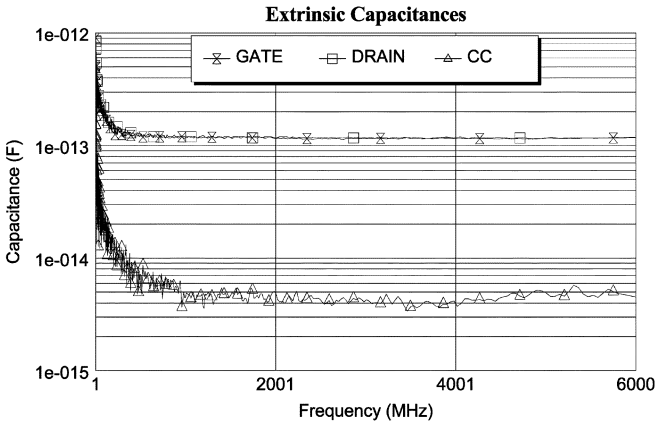

Fig. 7. Extrinsic bonding-pad capacitance extraction versus frequency.

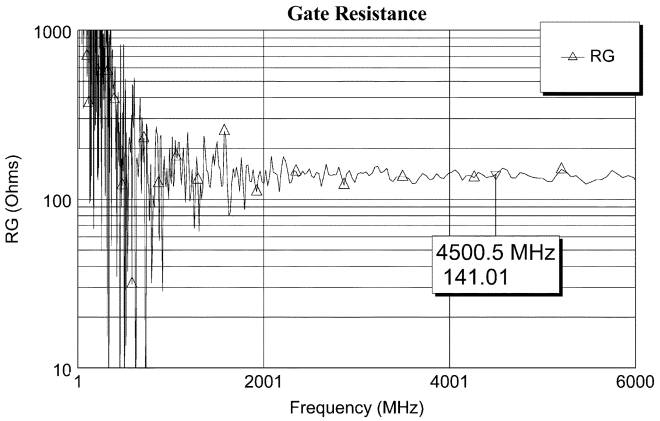

Fig. 8. Gate resistance extraction versus frequency. A mean extracted value of 141 Ω is shown.

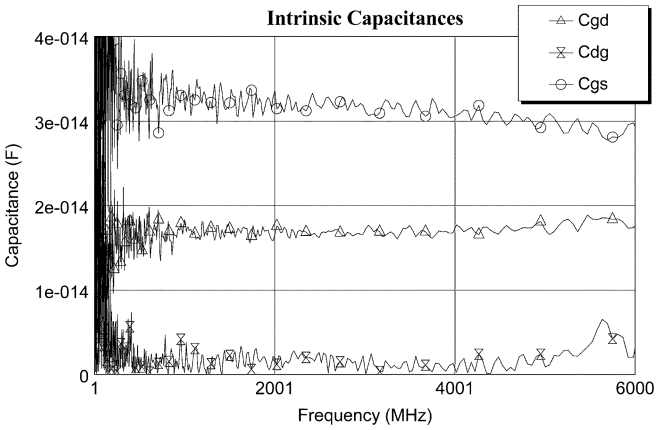

Fig. 9. Intrinsic capacitance extraction versus frequency.

Fig. 8 illustrates the extraction of the extrinsic resistance, $R_g(141\ \Omega)$, and the extraction of the intrinsic capacitances is shown in Fig. 9. These charts are included here as the relative constancy of the values extracted attests to the adequacy of the de-embedment and modeling procedure followed, as does the -20 dB/Dec plot of intrinsic $|\text{H21}|^2$ versus $\log(f)$ shown in Fig. 10. The plot of $|\text{H21}|^2$ versus $\log(f)$, computed from modeled intrinsic Y-parameter sets $|H_{21}|^2 = (Y21ix/Y11ix)$, also gives a clear -20 dB/Dec slope and this further attests to the quality of the modeling process. The bias scheme was chosen to ensure a useable micropower bandwidth where $g_m \geq g_{\rm ds}$ and

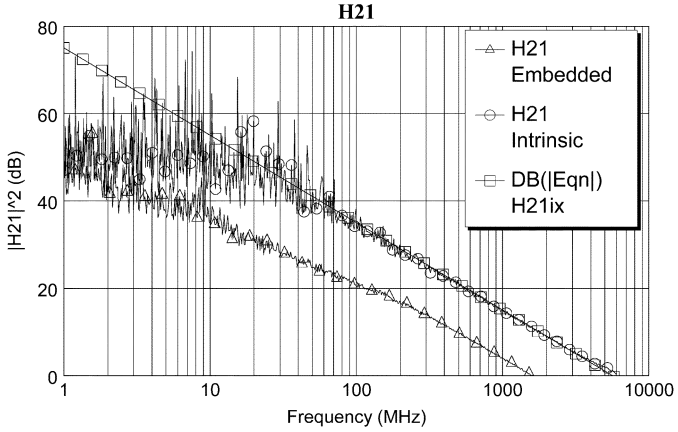

Fig. 10. Current gain $|H21|^2$ versus $\log(f)$. Embedded, extracted intrinsic and computed intrinsic ($\mathrm{H21_{ix}}$) plots are included.

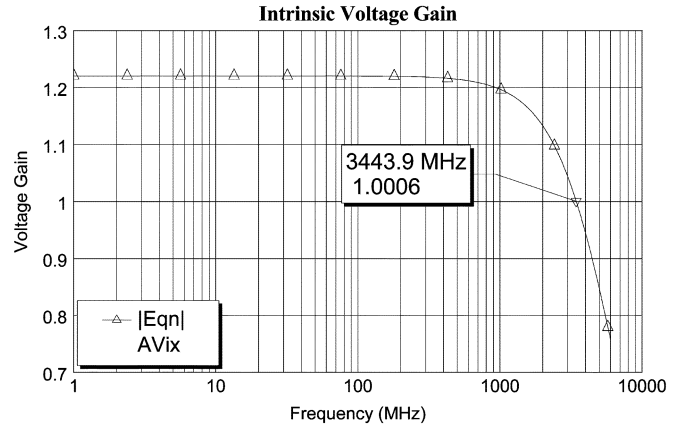

Fig. 11. Intrinsic voltage gain versus $\log(f)$. A unity-gain bandwidth of almost 3.5 GHz is notable.

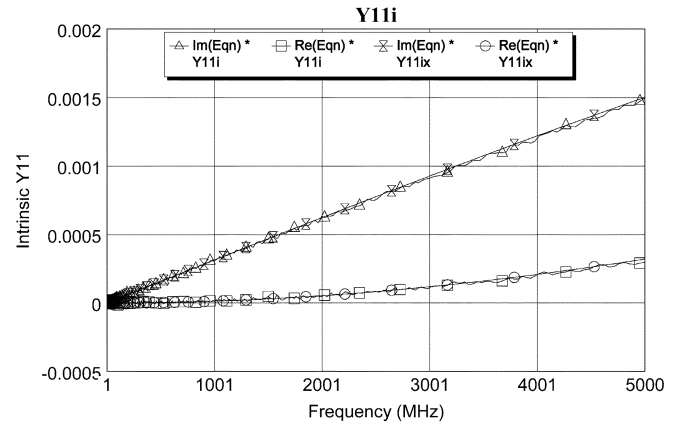

Fig. 12. Intrinsic device Y11 measured $(\mathrm{Y11_i})$ versus modeled $(\mathrm{Y11_{ix}})$.

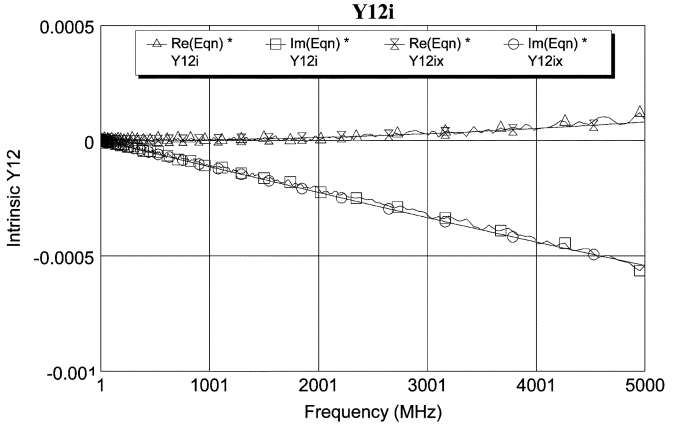

Fig. 13. Intrinsic device Y12 measured $(\mathrm{Y12_i})$ versus modeled $(\mathrm{Y12_{ix}})$.

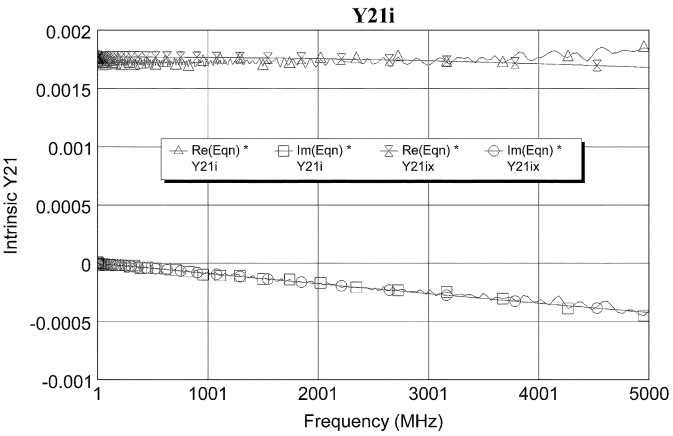

Fig. 14. Intrinsic device Y21 measured $(\mathrm{Y21_i})$ versus modeled $(\mathrm{Y21_{ix}})$.

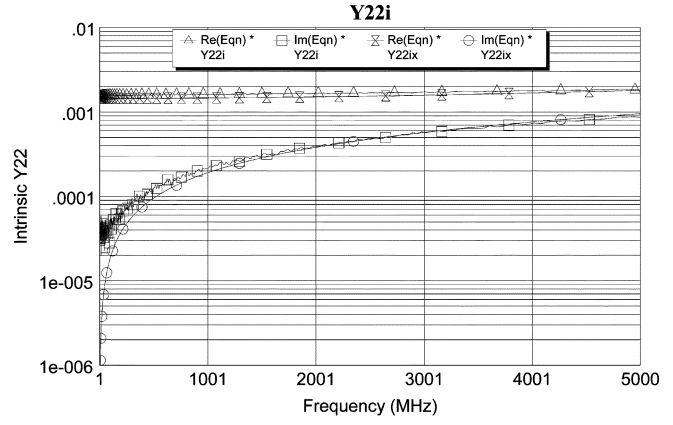

Fig. 15. Intrinsic device Y22 measured $(\mathrm{Y22_i})$ versus modeled $(\mathrm{Y22_{ix}})$.

the plot of intrinsic voltage gain $A_V = (Y21_i/Y22_i)$, given in Fig. 11, shows a unity-gain bandwidth of $\sim$3.5 GHz. It is worth noting that the access resistances contribute roughly 9% of the total channel resistance $(r_{\mathrm{ds}} = (1/g_{\mathrm{ds}}) = 667\ \Omega; \mathrm{RD} + \mathrm{RS} \approx 60\ \Omega)$ and that as these are not part of the KAIST model, they can be expected to cause a small degree of error, but this error is expected to decrease as the technology improves and access resistance mean values are reduced.

Figs. 12–15 are the measured versus modeled intrinsic Y parameters, and a good similarity is evident in most, the greatest error resulting in the real part of Y21 above 3.5 GHz, where $g_m < g_{\mathrm{ds}}$, and in the imaginary part of Y22 at low frequencies, due to a combination of current leakage and the fact that Y22 will be affected most by the effects of the total access resistance as both RS and RD form part of $\mathrm{Y22}^{-1}$. There is, in general, a good match at all frequencies below 3.5 GHz and as the bandwidth of any circuit employing these devices under micropower bias is unlikely to exceed this frequency, the model is acceptable for micropower RF design. A summary of all the extracted parameters is presented in Table I.

TABLE I
EXRACTED MODEL PARAMETERS

Parameter	Value
CpadG	115 fF
CpadD	115 fF
PadCC	4.8 fF
R_g	141 Ω
C_{gs}	32 fF
C_{gd}	17 fF
C_{dg}	2 fF
C_{sd}	- 1.3 fF
C_{jd}	9 fF
g_{ds}	1.5 mS
g_m	1.77 mS
R_{subd}	70 Ω

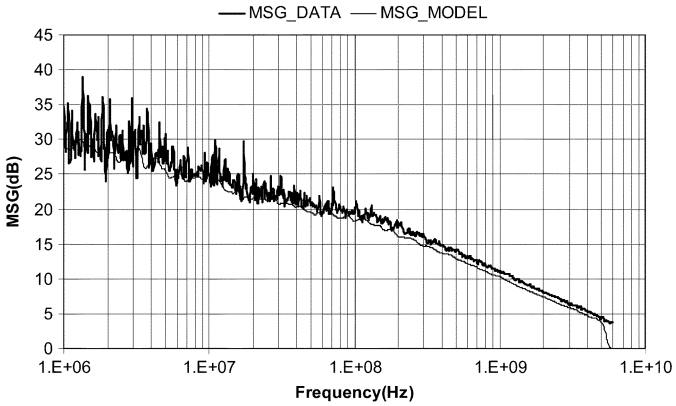

Fig. 16. MSG measured versus modeled.

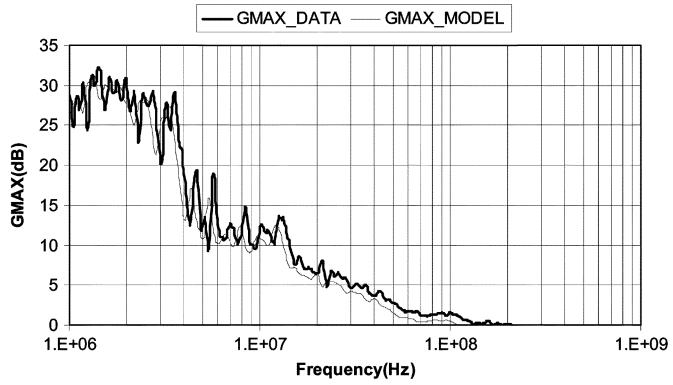

Fig. 17. G_{MAX} measured versus modeled.

B. Micropower Amplifier

The simulations in Figs. 16, and 17, show that a maximum power gain of 30 dB for G_{MAX} and 32 dB for MSG, together with a nonimpedance matched bandwidth of around 100 MHz, is achievable at the chosen micropower bias levels and the amplifier measured response reflects the simulated trends closely.

IV. CONCLUSION

The RF characteristics of a novel SiGe n-HMODFET operated at micropower levels with total power $= 294\ \mu$W have been successfully fit to the KAIST small-signal model, and all related extracted model parameters have been presented here for the first time. The model has then been used to simulate the performance of a realized SiGe micropower amplifier using a similar device and the measured versus simulated power gain and bandwidth comparison presented prove that this model is suitable for use in small-signal RF micropower simulations of HMODFET devices.

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