

SYSTEMATIC SYNTHESIS METHOD FOR ANALOGUE CIRCUITS – PART III ALL-TRANSISTOR CIRCUIT SYNTHESIS

David Haigh, Fang Qun Tan and Christos Papavassiliou

Electrical & Electronic Engineering Dept, Imperial College of Science Technology and Medicine, London SW7 2BT, UK

ABSTRACT

This paper and its companion papers (subtitled Parts I and II) together present a systematic synthesis method for analogue circuits. This paper illustrates the synthesis method by deriving and analysing some known all-transistor circuits from their specification matrices. Alternative circuits with better performance are obtained by introducing nullors which are equivalent to open- and short-circuits into the initial circuit. Nullors are replaced by simple equivalent circuits of transistors and non-ideal performance is evaluated. The synthesis method is shown to be a powerful tool which should be capable of generating novel all-transistor circuit solutions from given performance specifications.

1 INTRODUCTION

In a companion paper (Part I Notation and synthesis toolbox), the foundations for the systematic synthesis method to be applied in this paper were laid down [1], including a new admittance matrix notation for the ideal nullor using unbounded elements and admittance matrix representations for all types of controlled sources and the impedance converter using similar unbounded elements. In a second companion paper, the application of the method to synthesise active-RC circuits was explored [2]. In the context of analogue VLSI, high precision RC networks are difficult to realise and transistor-only circuits in which transfer function parameters depend on ratios of transistor parameters are of considerable interest [3,4]. The purpose of this paper is to illustrate the possibility of systematic synthesis for such all-transistor circuits. In this paper, we will assume the notation for admittance matrix description of nullor circuits in [1], the admittance matrix expansions for key circuit functions and definitions of such aspects as core matrix and matrix equivalence. We shall also make use of the V-7 transformation for pairs of nullators or norators which share a common terminal [1]. An important aspect of the synthesis method is the possibility of generating from an initial circuit equivalent circuits of greater complexity with a view towards obtaining better performance. This aspect of the synthesis method will be illustrated using examples.

In this paper, we begin by synthesising the open-circuit and the short-circuit using nullors. We then show how nullor open-circuits and short-circuits may be introduced into a circuit without affecting matrix equivalence. We then apply this synthesis concept to the operational transconductance amplifier and the current mirror to obtain several equivalent versions of each building block. Finally, we illustrate the replacement of the nullors by simple transistor equivalent circuits which allows evaluation of non-ideal performance.

2 OPEN-CIRCUIT AND SHORT-CIRCUIT

We first consider the synthesis of the open-circuit and the short-circuit from their admittance descriptions using nullors.

For the open-circuit, pivotal expansion [1] may be used to derive two nullor equivalents to the admittance description, shown using both ∞_i and bracket-type nullor notations [1]:

$$\begin{aligned}
 [0] &= \left[\begin{array}{c|c} 0 & 0 \\ \hline \infty_1 & -1 \end{array} \right] \mid \left[\overline{\begin{array}{c|c} 0 & 0 \\ \hline \infty_1 & -1 \end{array}} \right] \\
 [0] &\mid \left[\begin{array}{c|c|c} 0 & | & 1 \\ \hline 0 & | & 1 \end{array} \right] \mid \left[\overline{\begin{array}{c|c|c} 0 & | & 1 \\ \hline 0 & | & 1 \end{array}} \right]
 \end{aligned} \tag{1}$$

Both realisations comprise a series combination of a nullator and a norator connected between nodes 1 and 0 with node 2 the intermediate node.

For the short-circuit, the admittance description is:

$$[\infty_1] = \left[\overline{[\infty_1]} \right] \tag{2}$$

$[\infty_1]$ directly describes the circuit, namely a grounded nullator at node 1 and a grounded norator at node 1. The next step is to replace the nullor by a short circuit. This example shows the natural relationship between the use of specification Y-matrices with unbounded elements and the use of unbounded elements to describe nullors.

3 NULLOR INTRODUCTION

We now illustrate the introduction of nullors into a circuit using the admittance matrix representation. A series combination of a nullator and norator, a nullor open-circuit, may be connected between any two nodes of a circuit to produce an equivalent circuit. Let the two nodes of the circuit be i and j and let k be the new node, as shown in Fig 1(a). Then the Y -matrix is modified as shown using alternative nullor representations with introduction of extra row (k) and extra column (k):

$$\begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & y_{ij} & \cdot \\ \cdot & \cdot & \cdot \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & y_{ij} + \infty_1 & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & -1 & \cdot \\ \cdot & \cdot & -1 \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & y_{ij} & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \end{bmatrix} \quad (3)$$

Once the additional nullor is in place, any existing admittance terms may be moved between rows i and k and between columns j and k [2]. However, we should consider carefully the case when y_{ij} in 3 is an unbounded term ∞_2 representing an existing nullor; this situation is represented in eqn 4:

$$\begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & \pm\infty_2 & \cdot \\ \cdot & \cdot & \cdot \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & \pm\infty_2 + \infty_1 & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & -1 & \cdot \\ \cdot & \cdot & -1 \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & \pm\infty_2 + \infty_1 & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \end{bmatrix}$$

Now the V-7 transformation [1] may be used to show that the $\pm\infty_2$ term may be moved to row k and/or column k . Hence nullors may be introduced to expand a matrix by allowing existing nullor terms to be moved, just as if they were passive admittance terms. This is a technique which will be used in the next section to generate equivalent all-transistor circuits.

A nullor short-circuit, consisting of a parallel combination of a nullator and norator, may be connected in series with a passive element, a norator or a nullator to produce an equivalent circuit. Consider first the case of a passive element Y connected between nodes i and j with the nullor short-circuit inserted at node j and the additional node created denoted by k as shown in Fig 1(b). The admittance matrix is transformed as follows:

$$\begin{array}{c} i \quad j \\ \begin{bmatrix} \cdot & \cdot & \cdot \\ \cdot & Y & -Y \\ \cdot & -Y & Y \\ \cdot & \cdot & \cdot \end{bmatrix} = \begin{array}{c} i \quad j \quad k \\ \begin{bmatrix} \infty & \cdot & \cdot \\ \infty & Y & \cdot \\ \infty & \cdot & \infty_1 \\ \infty & \cdot & \cdot \\ \infty & \cdot & \cdot \\ \cdot & \infty Y & \infty_1 \end{bmatrix} \equiv Y \quad \begin{array}{c} \infty \\ \infty \\ \infty \\ \infty \\ \infty \\ Y + \infty_1 \end{array} \end{array} \end{array} \quad (5)$$

The Y terms in row j and column j have been moved to row and column k and node k is linked to node j by both a nullator and a norator.

Consider now the addition of a nullor short circuit in series with an existing norator connected between nodes i

and j . The connection of the norator to j is shifted to new node k and node k is linked to node j by both a nullator and a norator as shown:

$$\begin{bmatrix} \cdot & \cdot \\ \cdot & j \\ \cdot & k \end{bmatrix} = \begin{bmatrix} \cdot & \cdot \\ \cdot & i \\ \cdot & j \\ \cdot & k \\ \cdot & \cdot \\ \cdot & \cdot \end{bmatrix} \quad (6)$$

The V-7 transformation may be used to rearrange the connections of the two norators linking nodes i , j and k in any of 3 equivalent ways.

The insertion of a short-circuit nullor in series with a nullator is illustrated.

$$\begin{bmatrix} \cdot & \cdot \\ \cdot & m \\ \cdot & n \end{bmatrix} = \begin{bmatrix} \cdot & \cdot \\ \cdot & m \\ \cdot & n \\ \cdot & k \\ \cdot & \cdot \\ \cdot & \cdot \end{bmatrix} \quad (7)$$

Again, the V-7 transformation may be used to rearrange the connections of the two nullators linking nodes m , n and k in any of 3 equivalent ways.

Thus insertion of both the nullor open-circuit and short-circuit may be used to expand nullor circuits to obtain equivalent circuits.

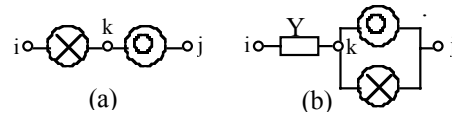


Fig 1: (a) Nullor open-circuit (b) Nullor short-circuit

4 TRANSCONDUCTOR EXAMPLE

The circuits we have synthesised in [2] contain nullors and passive elements. The usual approach for such circuits would be to arrange that the transfer function coefficients are determined by the passive elements and the nullors would be replaced by op-amps or transistors which approximate ideal nullors. However, an important class of circuits, particularly for analogue VLSI design, relies on ratios of transistor parameters to implement the transfer function. In this section and the next one, we consider two examples of all-transistor circuit synthesis, the operational transconductance amplifier and the current mirror.

The ideal operational transconductance amplifier can be represented by the admittance matrix of an ideal nullor:

$$\begin{bmatrix} 0 & 0 \\ \infty_1 & 0 \end{bmatrix} \equiv \begin{bmatrix} \overline{0 & 0} \\ 0 & 0 \end{bmatrix} \quad (8)$$

The circuit consists of a grounded norator at node 2 and a grounded nullator at node 1. Let us insert a nullor short circuit in series with the norator ground connection. We obtain the following, using both representations:

$$\begin{bmatrix} \overline{0 & 0 & 0} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \infty_2 \\ \infty_1 & 0 & \infty_2 \end{bmatrix} \quad (9)$$

We have moved the norator ground connection to new node 3 and connected node 3 to ground with both nullator and norator.

Finally, let us add a nullor open-circuit between node 3 and ground (4 is the new node). We obtain the following:

$$\begin{bmatrix} \overline{0 & 0 & 0 & 0} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \infty_3 & \infty_3 \\ \infty_1 & 0 & \infty_3 & \infty_3 \\ 0 & 0 & \infty_2 & 0 \end{bmatrix} \quad (10)$$

We have linked node 3 to 4 with a nullator and node 4 to ground with a norator.

The schematics for the circuits in eqns 8, 9 and 10 are shown in Fig 2; it can be seen that they are familiar forms of transconductance, basic, cascode and regulated cascode.

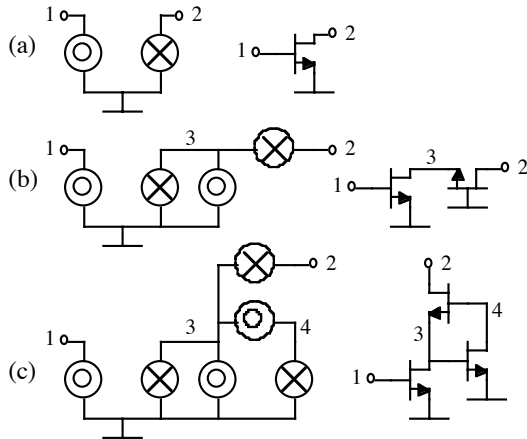


Fig 2: Operational transconductance amplifiers – (a) Basic (b) Cascode (c) Regulated cascode

Having derived the ideal equivalent circuits, we can now introduce non-ideal transistor parameters. For each nullor the ideal gain ∞_i may be replaced by a finite gain G . For nullor output nodes of k and l , we can introduce finite output conductance terms $y_{kk} = y_{ll} = g$, $y_{kl} = y_{lk} = -g$. For the three transconductor circuits derived, the corresponding Y-matrices are shown in Table 1. We also

show the Gaussian reduced 2×2 Y-matrix and the open-circuit gain expressions. By including the gate-source capacitance of the transistors, bandwidth and stability performance of the circuits could be compared.

Table 1: Non-ideal analysis of transconductance amplifiers

	Simple	Cascode	Regulated cascode
Y	$\begin{bmatrix} 0 & 0 \\ G & g \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 \\ 0 & g & -G-g \\ G & -g & G+2g \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & g & -G-g & G \\ G & -g & G+2g & -G \\ 0 & 0 & G & g \end{bmatrix}$
$Y_{2 \times 2}$	$\begin{bmatrix} 0 & 0 \\ G & g \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 \\ G(G+g) & g^2 & 0 \\ D_2 & D_2 & 0 \\ 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ G(G^2+Gg+g^2) & g^3 & 0 & 0 \\ D_3 & D_3 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$
$A_V = \frac{y_{21}}{y_{22}}$	$-\frac{G}{g}$	$-\left(\frac{G}{g}\right)^2 \mid \frac{G}{g}$	$-\left(\frac{G}{g}\right)^3 \mid -\frac{G}{g} \mid -\frac{G}{g}$

5 CURRENT MIRROR EXAMPLE

As another example of a family of all-transistor circuits with different levels of performance, we consider the current mirror. The 2×2 admittance matrix description for the CCCS with gain $A_1 = N/D$ derived in [1] is:

$$\begin{bmatrix} \infty_1 & 0 \\ A_1 \infty_1 & 0 \end{bmatrix} \equiv \begin{matrix} \equiv_1 & 0 \equiv \\ \equiv_2 & 0 \equiv \end{matrix} \equiv \begin{bmatrix} \overline{0 & 0} \\ 0 & 0 \end{bmatrix} \quad (11)$$

We adopt the approach of letting the term $A_1 \infty_1 = \infty_2$ where ∞_2 represents a second nullor. When the nullors are replaced by transistors ($\infty_1 \rightarrow G_1$, $\rightarrow \rightarrow G_2$), the current gain A_1 in eqn 11 corresponds to the ratio of the transistor gains (G_2/G_1) which is determined by the well-defined ratio of the transistor W/L ratios. The parameter \rightarrow on the other hand can be related to a parameter which affects both transistors equally, such as oxide thickness.

The second expression in eqn 11 corresponds to the basic current mirror shown in Fig 3(a). Note that this example suggests that a parallel connection of two nullators should be treated as distinct from a single nullator.

Equation 11 also gives (on the right) the general nullator-norator representation for the current mirror. We now expand the circuit (and matrix) by introducing a new node 3 connected to ground by a short-circuit nullor; this allows us to reconnect two of the original ground connections to node 3 instead:

$$\left[\begin{array}{c|c|c} \hline \left[\begin{array}{c|c|c} \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline \end{array} \right] & & \\ \hline \end{array} \right] \equiv \left[\begin{array}{c|c|c} \hline \left[\begin{array}{c|c|c} \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline \end{array} \right] & & \\ \hline \end{array} \right] \equiv \left[\begin{array}{ccc|c} 0 & 0 & \infty_1 & \\ \infty_3 & 0 & -3 & \\ -3 & 0 & -2+3 & \end{array} \right] \quad (12)$$

Next we expand the circuit further by adding a 4th node:

$$\left[\begin{array}{c|c|c|c} \hline \left[\begin{array}{c|c|c|c} \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline \end{array} \right] & & & \\ \hline \end{array} \right] \equiv \left[\begin{array}{c|c|c|c} \hline \left[\begin{array}{c|c|c|c} \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline \end{array} \right] & & & \\ \hline \end{array} \right] \equiv \left[\begin{array}{ccc|c} \infty_3 & 0 & -3 & 0 \\ -4 & 0 & 0 & -4 \\ -3 & 0 & -1+3 & 0 \\ -4 & 0 & -2 & -4 \end{array} \right] \quad (13)$$

The 4th node is effectively a nullor short-circuit to ground and allows repositioning of one nullator and several norators.

The circuit diagrams corresponding to the matrices in eqns 12 and 13 are shown in Fig 3(b) and (c) and it can be seen that they are the Wilson and cascode current mirror, respectively.

In Table 2, we replace the ideal nullor models with simple equivalent circuits with finite gain G and output

conductance g . Then we reduce the matrices to 2×2 form and determine the output conductance for short-circuit excitation (y_{22}) and also for open-circuit excitation ($y_{00} = y_{22} - y_{12}y_{21}/y_{11}$). This analysis shows that the low output conductance of the Wilson current mirror is only obtained for high source impedance.

6 CONCLUSIONS

We have attempted to present a systematic synthesis method for analogue circuits and to illustrate its use for all-transistor circuits by the synthesis of some known example circuits. We have shown how alternative realisations which are equivalent assuming ideal nullors can be derived and also how equivalent circuits for real devices may be substituted for the nullors to assess performance. It is believed that this synthesis tool could facilitate the development of performance optimised circuits which fully takes into account the interaction between the elements at the initial design stage. We believe also that the synthesis method is a powerful tool capable of generating novel circuit solutions.

7 REFERENCES

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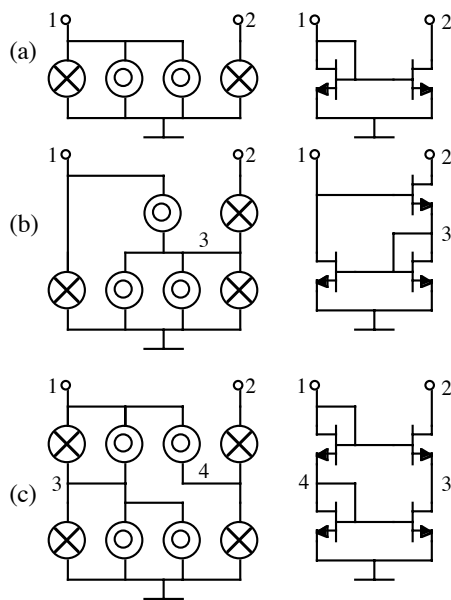


Fig 3: Current mirrors

(a) Simple (b) Wilson (c) Cascode

	Simple	Wilson	Cascode
Y	$\begin{bmatrix} G+g & 0 \\ G & g \end{bmatrix}$	$\left[\begin{array}{c c} g & 0 \\ \hline G & g \end{array} \middle \begin{array}{c} G \\ -G-g \end{array} \right]$	$\left[\begin{array}{c c c} G+g & 0 & -G-g \\ \hline G & g & 0 \\ \hline -G-g & 0 & 2G+2g \\ \hline -G & -g & G \end{array} \middle \begin{array}{c} 0 \\ -G-g \\ 0 \\ G+2g \end{array} \right]$
$Y_{2 \times 2}$	$\begin{bmatrix} G+g & 0 \\ G & g \end{bmatrix}$	$\left[\begin{array}{c c c} \frac{G^2+2Gg+2g^2}{2(G+g)} & \frac{Gg}{2(G+g)} & 0 \\ \hline G/2 & g/2 & 0 \\ \hline 0 & 0 & 0 \end{array} \right]$	$\left[\begin{array}{c c c c} (G+g)/2 & 0 & 0 & 0 \\ \hline G(G+3g) & g^2 & 0 & 0 \\ \hline 2(G+2g) & G+2g & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \end{array} \right]$
y_{22}	g	$\frac{g}{2}$	$\frac{g^2}{G+2g}$
y_{00}	g	$\frac{Gg^2+g^3}{G^2+2Gg+2g^2}$	$\frac{g^2}{G+2g}$

Table 2: Non-ideal analysis of current mirrors