A Monolithic 4×4 TIA, Crosspoint Switch and Laser Driver IC with Very High Programming Speed

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Abstract

A 4×4 optoelectronic crosspoint switch, designed for short-haul communication networks, with less than 1 ns programming time per channel is presented. The IC implements TIAs, switch core and laser drivers using a 0.8 μm SiGe HBT BiCMOS technology that is a commercially available and mature fabrication technology. The switch has a nonblocking architecture with broadcasting capability and asynchronous data paths. The simulation and experimental results of the chip, which employs the most recently proposed ideas for single-ended input to differential output conversion [1] and high-isolation multiplexing [2], are also presented.

1. Introduction

The demand for high-volume data transmission has greatly influenced the development of high-speed crosspoint switches. These important building blocks make connections between input and output channels in a typical communication network. Crosspoint switches are usually used in local- and wide- area networks both as a routing component and as a means for sharing expensive resources. They are also a key component in telecommunication central offices.

Since fibre optic links now dominate long- and short-haul data communication, a typical routing and amplification system consists of photodetectors, transimpedance amplifiers (TIAs), switch core, laser drivers and laser diodes.

This work concentrates on integrating the TIAs, switch core and laser drivers monolithically using a 0.8-μm SiGe HBT BiCMOS technology that is a commercially available and mature fabrication technology. The next stage of this work will concentrate on integrating the photodetector and laser diode as well.

Conceptually, an *n*×*n* crosspoint switch can be considered as a block with *n* input and *n* output lines arranged in a matrix form. In this matrix, as shown in Figure 1, a connection between each horizontal input line and vertical output line can be established by activating the switch located at the intersection of the input and output lines.

Since the overall data throughput and reliability in data communication systems are highly dependent on the performance of crosspoint switches within them, it is crucial that the problems involving their design be addressed carefully.

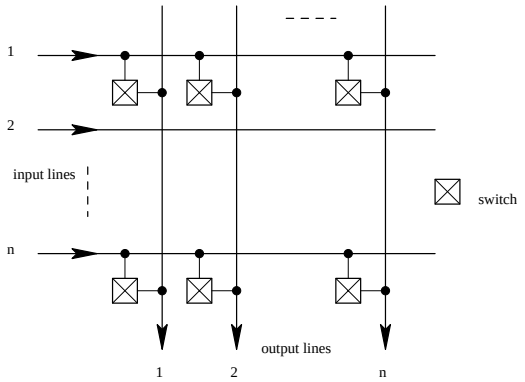

Figure 1. Crosspoint switch representation

2. Design considerations

For maximum flexibility, the crosspoint switch needs to be designed with the following figures of merit:

- Broadcasting ability, which means the possibility of establishing a connection between an input line and more than one output line at the same time.
- Nonblocking property, which means any specific connection between input and output lines does not prevent an input line from being connected to an idle output line.

Since the overall data throughput of any communication system depends on the bandwidth and signal-to-noise ratio (SNR) these two issues need to be considered carefully. Two important factors degrading SNR are the crosstalk between the channels and the random noise generated by the circuit elements such as transistors and resistors. Crosstalk is mainly due to intrinsic parasitic capacitances in active devices, parasitic capacitances between the interconnects, common power/ground lines, and coupling through the chip substrate. The amount of crosstalk can be reduced greatly by using complementary signals and deploying special architectures for the switch core section described later.

Apart from degrading SNR, crosstalk and noise cause some degree of randomness (called *timing jitter*) in zero-crossing time of the output signals. Since these output signals will be sampled by a decision circuit for being interpreted as "0" or "1" bits, this timing jitter may cause wrong decisions which eventually result in the increase of bit-error rate of the whole system.

Finally, reconfiguration (programming) time for establishing a new connection leads to loss of data, therefore, having a fast programming section is of paramount importance (especially for crosspoint switches that are used in high-speed ATM packet switching applications).

3. Circuit design

The block diagram of the $n \times n$ optoelectronic crosspoint switch using multiplexer/decoder architecture is shown in Figure 2. Two main parts of this architecture are the high-speed data path (from input to output) and the programming section. A single data path consists of a receiver, an n-to-1 multiplexer and a laser driver. As Figure 2 shows, there is a n-to-1 multiplexer associated with each output channel and since the outputs of the receiver stage are connected to the inputs of all multiplexers, this architecture clearly provides the broadcasting and non-blocking properties discussed before. An n-to-1 multiplexer requires $m = \log_2 n$ select lines which must be stored in an m-bit input-address latch. The output-address decoder selects one of n available input-address latches according to its $\log_2 n$-bit output-address inputs. After the appropriate input-address latch is selected, the setup will be completed by applying a single pulse on the *prg_en* line. Since each setup is separate and independent of others, the complete setup of all n output lines requires n *prg_en* pulses.

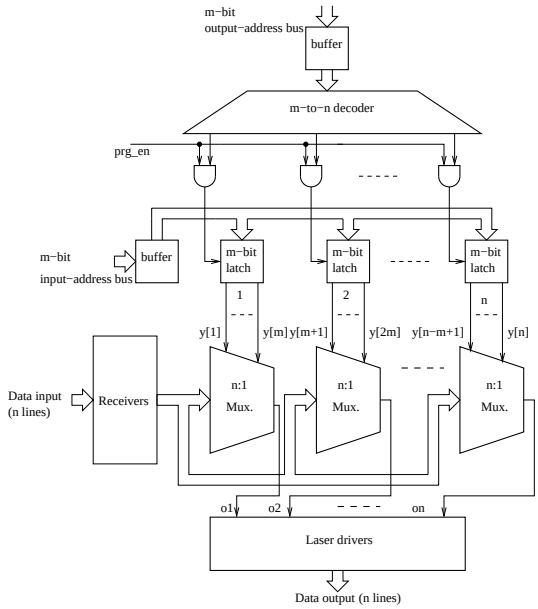

Figure 2. Block diagram of the multiplexer/decoder architecture for crosspoint switch

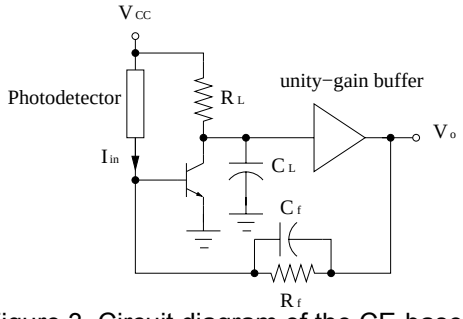

Figure 3. Circuit diagram of the CE-based transimpedance amplifier

3.1. Receivers

Speed and sensitivity are the two most important design goals in optoelectronic receivers. Sensitivity S_n, defined as the minimum detectable optical power, can be expressed as

$$S_n = \frac{\eta P_{opt}}{\sqrt{2}} = \frac{\hbar \nu}{q} \sqrt{\frac{S}{N}} \sqrt{\overline{i_n^2}} \qquad (1)$$

where

q : electron charge
$\hbar$: Plank's constant
ν : optical frequency
S/N : signal-to-noise ratio
$\overline{i_n^2}$: total input mean-square noise current

SNR is set by the desired bit-error rate (BER), defined as the probability of incorrect identification of a bit by the decision circuit of the receiver. Therefore, S_n will be determined by the optical frequency and total input mean-square noise current, which depends on the receiver circuit design and the technology in which it is implemented. At the heart of the receiver is a transimpedance amplifier which deploys shunt-shunt feedback to achieve low input and output impedances. Figure 3 shows a simplified circuit diagram of a CE-based TIA. The 3-dB bandwidth of this amplifier can be calculated as [3]

$$f_{-3dB} \approx \frac{1}{2\pi \sqrt{\dfrac{c_\pi + c_\mu (1 + g_m r_c) + c_p}{g_m} (c_\mu + c_L) R_f}} \qquad (2)$$

where c_π, c_μ, g_m, and r_c are part of the small-signal model of the transistor and c_p is the internal capacitance of the photodetector.

A detailed analysis [4] shows that $\overline{i_n^2}$ decreases as R_f increases which according to Equation (1) leads to improved sensitivity. However, according to Equation-(2) f_{-3dB} is inversely proportional to R_f. There will always, therefore, be a trade-off between sensitivity and bandwidth in the receiver design.

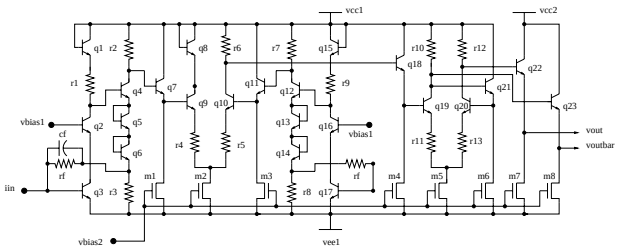

Figure 4. Receiver stage schematic

The complete circuit diagram of the receiver is shown in Figure 4. It consists of a TIA, a gain stage, and a single-ended input to differential output converter. The cascade amplifier is used instead of a common-emitter amplifier as it provides higher bandwidth. The feedback network incorporates capacitive compensation to implement the capacitive-peaking technique [5]. This is effectively a phase-log compensation improving the TIA bandwidth. TIA is followed by a gain stage in which a differential amplifier with emitter degeneration is employed. This differential amplifier provides a stabilised voltage gain and eliminates the need for a decoupling capacitor. The inactive input side of the differential amplifier is connected to the output of a dummy TIA stage which results in a balance between the dc voltages at both the inputs of the gain stage. This gain stage is followed by a MFECL gate [1] to provide the two complementary ECL-compatible output signals required by the rest of the crosspoint switch. Moreover, it eliminated the need for a limiting amplifier.

3.2. Multiplexers

To minimise the inter-channel crosstalk, a modified 4-to-1 multiplexer architecture based on the multiplexer proposed in [2] is used in the switch matrix core section. As shown in Figure 5, this multiplexer consists of two stages, both controlled by a current steering tree. The second stage is a conventional ECL multiplexer, but the first stage provides the extra isolation by switching differential buffers.

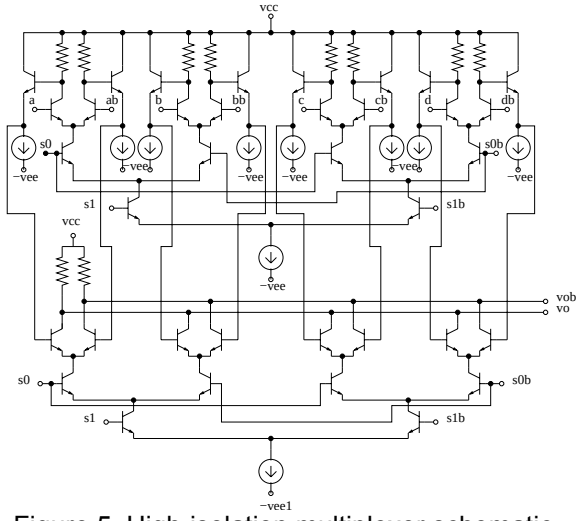

Figure 5. High-isolation multiplexer schematic

The conventional ECL multiplexer suffers from crosstalk due to the presence of switching signals on adjacent channels. However, in the high-isolation multiplexer, non-selected inputs are shielded from capacitively-coupled noise through the non-selected buffer pairs. Simulation results show this coupled noise improves from -30 dB to -50 dB at 2 Gb/s data rate.

3.3. Laser drivers

Figure 6 shows the schematic diagram of the laser driver. Laser drivers have been optimised to drive VCSEL arrays with shared grounded cathodes. The modulation current can be controlled externally between 0 to around 10 mA depending upon the requirement. Buffers are used at the input to enable the multiplexers to drive the large transistors of the laser drivers. These buffers have been appropriately biased to minimise ringing while maintaining a reasonable rise/fall time. Separate V_{CC} and V_{EE} pads are used for every laser driver to minimise crosstalk.

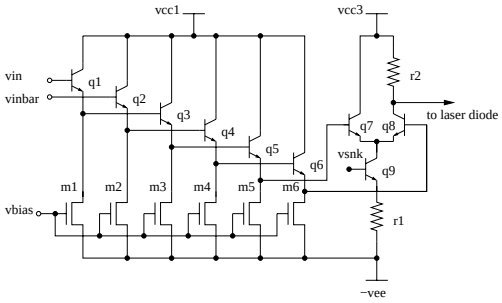

Figure 6. Laser driver schematic

4. Results

Both, the simulation and experimental results are presented here. The 4×4 crosspoint switch was simulated using Cadence Spectre simulator. Figure 7 shows the simulation result for the laser driver currents (outputs of the circuit). Programming time can be estimated as the time it takes from applying the *prg_en* signal, to establishing a bias current in the data-path-differential pairs of the multiplexer. Figure 8 shows the simulation result for the chip reconfiguration time per channel. A summary of the simulation results for the main parameters of the chip is displayed in Table 1.

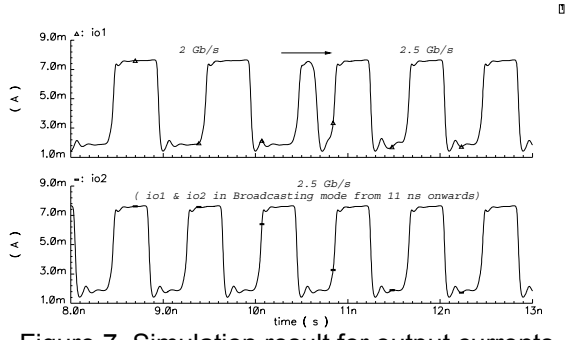

Figure 7. Simulation result for output currents

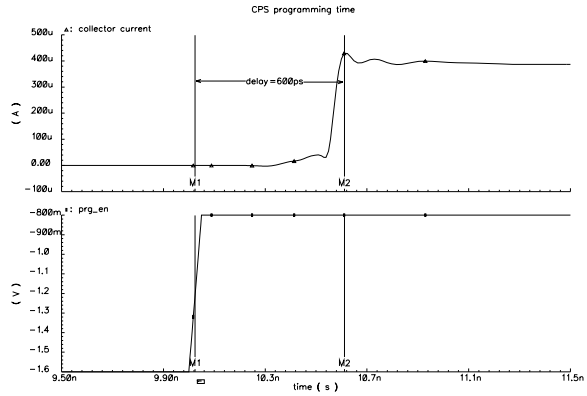

Figure 8. Simulation result for programming time

Experimental results were obtained using a probe card to supply the power and programming signals. The high-speed data inputs and outputs were probed using G-S-G air coplanar probes (with 40 GHz bandwidth). Due to the equipment, only one input and one output could be tested simultaneously. A 1 GHz signal generator was used to provide the input signal, and the output was viewed on a 1 GHz bandwidth oscilloscope. Figure 9 shows the eye diagram with 1 Gbps data rate and 88 ps timing jitter. Figure 10 shows the die photo of the optoelectronic crosspoint switch. The data inputs are on the left and outputs on the right, and both use a G-S-G pattern to provide extra siolation.

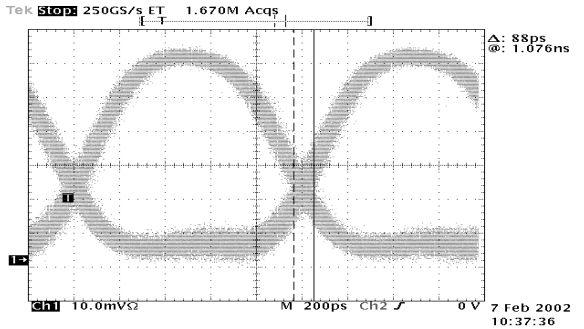

Figure 9. Output eye diagram at 1 Gb/s

5. Conclusions

Using AMS 0.8 μm SiGe HBT BiCMOS technology that is a commercially available and mature fabrication technology, a monolithic 2.5 Gb/s/channel 4×4 opto-electronics crosspoint switch with very high speed of programming (< 1 ns per channel) is presented. This chip can be readily used in ATM packet switching and SONET applications.

6. Acknowledgements

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Table 1. Values of main parameters of the chip

Technology	0.8 μm HBT BiCMOS
Chip area	1.6 mm × 2.3 mm
Chip size	4×4
Data rate	0–2.5 Gb/s
Chip delay	422 ps
Programming time per channel	< 1 ns
Current sensitivity	25 μA
Control signals logic	ECL
Power supplies	-5, -1 V
Power consumption including laser drivers	820 mW

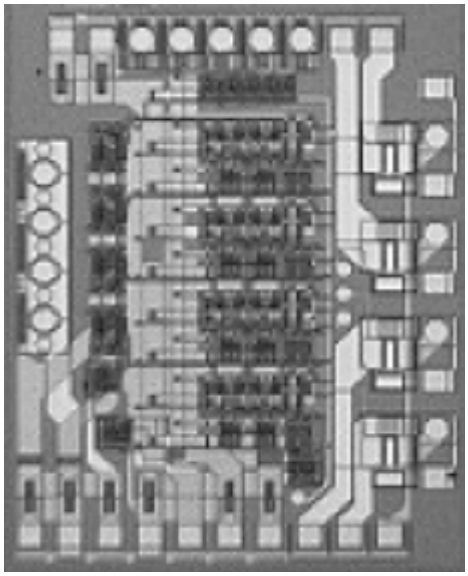
Figure 10. Die photograph of the 4×4 optoelectronic crosspoint switch

7. References

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