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SiGe virtual substrate HMOS transistor for analogue applications

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Abstract

Silicon–germanium (SiGe) heterojunction metal-oxide-semiconductor field-effect transistors (SiGe HMOSFETs) have been successfully fabricated on Si substrate. The semiconductor heterostructure, which was grown by gas-source molecular beam epitaxy (GS-MBE), was initiated by the deposition of a $Si_{0.7}Ge_{0.3}$ "virtual substrate". The n-type transistors were fabricated using a standard MOS process. The channel is a thin, undoped layer of strained Si and is buried below an arsenic-doped $Si_{0.7}Ge_{0.3}$ layer, which provides the carriers. The devices exhibited excellent current–voltage (I–V) characteristics in terms of transconductance and drain current, with no breakdown or leakage. A level-1 model was extracted, for use in circuit design. The results suggest that the realisation of buried-channel SiGe n-HMOSFETs is feasible in MOS processes. These devices are of particular importance in analogue applications.

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1. Introduction

The Si/silicon–germanium (SiGe) heterojunctions became popular during the 1990s, when Ge was introduced, to realise heterojunctions in the silicon base of bipolar transistors (HBTs). This offered the advantages of higher f_T (50 GHz) and lower base resistance, resulting in lower transmit noise and higher receiver sensitivity (several emerging applications use carrier frequencies up to 5 GHz, requiring transistor f_T of 50 GHz) [1]. But with CMOS remaining the dominant technology, the Si metal-oxide-semiconductor field-effect transistor (MOSFET) is being continuously scaled down and fundamental limits are being reached. It is therefore wise to investigate new technologies. In the International Technology Roadmap for Semiconductors [2], non-classical CMOS and band-engineered transistors are tabulated under the "near future" timing, referring to structures with SiGe or strained-Si channels on bulk Si or silicon on insulator (SOI) substrates. In addition to the processing compatibility with CMOS, SiGe HMOS transistors have much more to offer: first, higher drive current and speed, which arise from the strained channels. Then, it is mobility enhancement, especially in p-channel devices [3], which promises a truly complementary process and is of particular importance to digital circuits. Low noise operation is achievable, due to the buried channels that can be realised. And last, but not least, SiGe HMOS transistors have a huge

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potential in the fields of RF analogue electronics and micropower applications. The research has benefited a lot from the advances in SiGe heterojunction FETs (HFETs) [4], where n-channel devices have figures of merit comparable to similar geometry GaAs transistors. It is emphasised here, that these devices too have buried channels (but not a gate oxide). Reported experimental Si/SiGe n-channel HMOS data are limited [5] and the trend is towards surface channel devices and not buried channel. Furthermore, the performance remains below the theoretical predictions [6].

2. Experimental details

All epilayer growth (Fig. 1) was carried out by gas-source molecular beam epitaxy (GS-MBE), using fluxes of disilane (Si_2H_6) and germane (GeH_4) at 550 °C. The pressure during growth was maintained in the range of 10^{-5} to 10^{-4} T. The initial material was a high-resistivity p-type B-doped Si substrate. First, a graded-composition SiGe layer was deposited, followed by a relaxed p-type $Si_{0.7}Ge_{0.3}$ virtual substrate. The top 100 nm of the virtual substrate were B-doped at a lower level, to minimise the inverted substrate charge. The nominally 8 nm thick strained-Si channel was then grown, free of any intentional dopants. An arsenic-doped (1×10^{18} cm^{-3}), 10 nm thick $Si_{0.7}Ge_{0.3}$ donor layer then followed. This layer engineers the band gap discontinuity and donates the electron carriers to the resulting channel, within the strained-Si layer. Finally, a 10 nm undoped silicon layer was grown on top of the structure. This is consumed during transistor fabrication, to form the gate oxide, as in conventional MOSFETs.

The fabrication of the transistors was performed as follows: initially, electrical isolation of the individual devices from within the epitaxial layers was required (MESA isolation). This was done by chemically removing the active epitaxial material around the transistors to a depth of 300 nm (down to the virtual buffer layer). MESA isolation of active devices is common practice in doped epitaxial structures. Then, a standard Si MOS process was carried out with reduced thermal loads, where possible, in order to maintain the strain and reduce Ge diffusion in the device channel. MOS device isolation, in particular, consisted of 300 nm low-temperature oxide (LTO), deposited at 400 °C, in which, active areas were defined by patterning and etching, using a BHF solution. Dry thermal oxidation at 800 °C for 60 min was used to grow the gate oxide (resulted thickness 6 nm). Amorphous Si (300 nm) was deposited and implanted with As (1×10^{15} cm^{-2}, 40 keV). Rapid thermal annealing (RTA) was performed at 800 °C for 30 s in order to activate the resulting poly Si for gate definition, which was carried out using electron beam

10 nm	Si (undoped)	cap layer
10 nm	$Si_{0.7}Ge_{0.3}$ n = 1x10^{18} cm^{-3}	donor layer
5 nm	$Si_{0.7}Ge_{0.3}$ (undoped)	spacer layer
8 nm	Si **Channel** (undoped)	(strained)
100 nm	$Si_{0.7}Ge_{0.3}$ (undoped)	spacer layer
100 nm	$Si_{0.7}Ge_{0.3}$ p = 5x10^{16} cm^{-3}	
1μm	$Si_{0.7}Ge_{0.3}$ **Virtual Substrate** p = 5x10^{17} cm^{-3}	
1μm	$Si_{1-x}Ge_x$ x = 0 –32 % p = 5x10^{17} cm^{-3}	
	p-type Si substrate	

Fig. 1. The SiGe HMOS layer structure. All shown parameters are nominal.

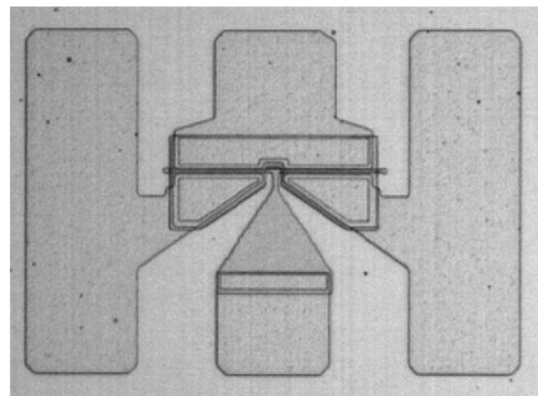

Fig. 2. Optical microscope image of a transistor intended for high-frequency on-wafer characterisation. The distance between adjacent contact pads is 100 μm.

lithography. Dry etching the poly produced gate lengths down to 300 nm and was followed by self-aligned source and drain implants using As (5×10^{15} cm^{-2}, 40 keV). A 30 s RTA at 825 °C was used for implant activation. The interlayer dielectric (ILD) consisted of 100 nm LTO (400 °C), followed by 200 nm of BPSG. Contact vias were then dry etched through the ILD. The metalization system consisted of sputtered Al (1% Si) with a Ti barrier layer. A microscope image of a device intended for RF on-wafer measurements is shown in Fig. 2.

3. Measurements and discussion

After fabrication, a number of transistors with different geometries were available on-wafer for characterisation. The shortest gate length was 300 nm, with a gate width of 100 μm. Typical dc characterisation results from these devices appear in Figs. 3–5. The current–voltage characteristics are shown in Fig. 3 (solid curves). The transistor turns properly off for gate voltages below 0.4 V and shows no breakdown for drain voltages up to 1.5 V. A standard level-1 NMOS PSPICE model was extracted, for use in circuit design. The modelled dc *I–V* characteristics are shown as dots in Fig. 3. The fit was accomplished by optimising the simulated data (in Microwave Office CAD software) versus the measured dc data. The extracted parameters are listed in the insert, in standard level-1 notation and units. This model can adequately cater for the dc performance of analogue circuits, but further work is underway for the implementation of a more appropriate tool, which takes into account the full nature of a buried-channel heterojunction MOSFET.

The measured current transfer characteristics at saturation are presented in Fig. 4. The maximum transconductance is 200 mS/mm and the corresponding drain current is in excess of 220 mA/mm, reaching up to 380 mA/mm at high overdrive. The wide maximum, which occurs with respect to V_{GS}, can be attributed to the presence of mobile carriers in both the channel and the donor layer. This is of particular importance for analogue circuit design, since part of

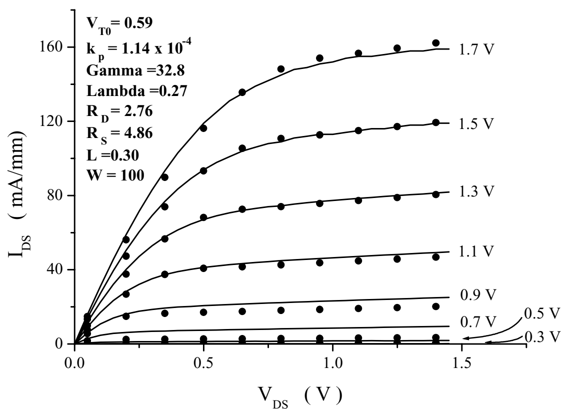

Fig. 3. Typical current–voltage characteristics (solid curves) of a transistor with gate length of 0.3 μm and width of 100 μm. The V_{GS} values are shown next to the corresponding curves. The extracted level-1 model (see insert) is represented by the dots.

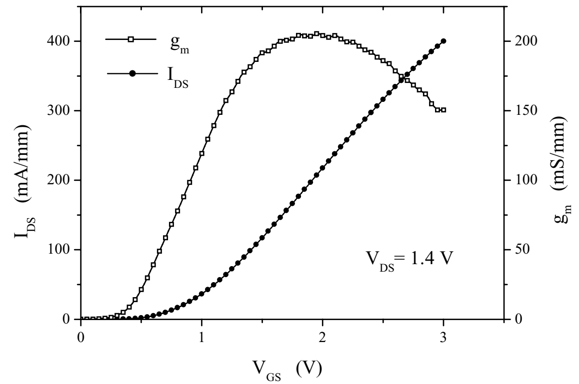

Fig. 4. The transfer characteristics of the device of Fig. 3 (at saturation).

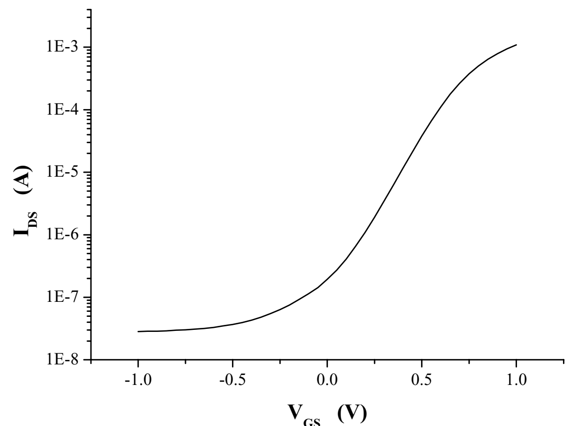

Fig. 5. Sub-threshold characteristics at $V_{DS} = 0.1$ V. The sub-threshold slope is 200 mV per decade.

the transistor power can be intentionally traded-off with linearity, by proper structure engineering. Fig. 5 shows the I_{DS} versus V_{GS} characteristics, which are of importance for micropower applications. The device exhibits an off-state current of 30 nA and a sub-threshold slope of 200 mV per decade. The V_{DS} was 0.1 V.

The RF performance of the 0.5 μm long-gate devices of Fig. 2, was measured on-wafer, using a HP 8753D network analyser. From these measurements, a non de-embedded cut-off frequency of 550 MHz was extracted. This relatively poor RF performance could be partly attributed to crystal defects, which may have degraded the quality of the strained material. Although no independent characterisation (i.e. TEM) is available to verify this claim, such defects are known to pose a problem and can be reduced with further optimisation of the epitaxial growth [7]. Nonetheless, combined low-V_{DS} I–V and C–V measurements on long-gate FETs, yielded a drift channel mobility of 20 $cm^2/(V\ s)$, at room temperature, indicating that the material quality could, indeed, be an issue.

4. Conclusion

Buried-channel SiGe n-HMOSFETs have a huge potential for modern RF analogue circuit design. They are superior to their conventional Si counterparts, in terms of the usual trade-offs between power, speed, linearity and noise. The results of this work show that their incorporation in CMOS processes is feasible and that, surface-channel devices are not the only way forward.

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References

[1] J. Sevenhans, F. Op't Eynde, P. Reusens, IEEE Trans. Microwave Theory Tech. 50 (1) (2002) 235.
[2] International Sematech, International Technology Roadmap for Semiconductors, 2001 (Semiconductor Industry Association, 2001).
[3] M.J. Prest, et al., Mater. Sci. Eng. B 89 (2002) 444.
[4] M. Zeuner, A. Fox, T. Hackbarth, D. Behammer, U. Koenig, in: Proceedings of the 60th Device Research Conference Digest, 2002, p. 53.
[5] K. Rim, in: Proceedings of the Solid-State Circuits Conference on Digest of Technical Papers (ISSCC, IEEE International), 2001, p. 116.
[6] A.G. O'Neill, D.A. Antoniadis, IEEE Trans. Electron Device 43 (1996) 911.
[7] S.H. Olsen, A.G. O'Neill, D.J. Norris, A.G. Cullis, N.J. Woods, J. Zhang, K. Fobelets, H.A. Kemhadjian, Semicond. Sci. Technol. 17 (2002) 655.