Available online at www.sciencedirect.com
SCIENCE DIRECT®
Applied Surface Science 224 (2004) 390–393
applied surface science
www.elsevier.com/locate/apsusc

Effect of temperature on the transfer characteristic of a 0.5 μm-gate Si:SiGe depletion-mode n-MODFET

V. Gaspari[a,*], K. Fobelets[a], J.E. Velazquez-Perez[b], R. Ferguson[a], K. Michelakis[a], S. Despotopoulos[a], C. Papavassilliou[a]

[a]*Department of Electrical and Electronic Engineering, Imperial College London, Exhibition Road, SW7 2BT London, UK*
[b]*Departamento de Fisica Aplicada, Universidad de Salamanca, Edificio Trilingue, Pza. de la Merced s/n, 37008 Salamanca, Spain*

Abstract

An investigation of the low-temperature operation of a 0.5 μm-gate Si:SiGe depletion-mode n-type modulation-doped field-effect transistor is presented. The investigated temperatures range from $T = 300$ to 180 K. The benefits of cryogenic operation are discussed. Experimental indications of parallel conduction in the device are presented, as well as their dependence on operating temperature. Measured data are compared with two-dimensional device simulations in MEDICI™ carried out using mobility values from Monte Carlo material calculations.

PACS: 71.20.Nr; 73.40; 73.40.Qv; 85.30.Tv; 85.40.-e; 07.20.M

Keywords: Semiconductor compounds; Heterostructures—electrical properties; Metal–insulator–semiconductor structures (including semiconductor-to-insulator); Field-effect devices; Microelectronics: LSI, VLSI, ULSI; Integrated circuit fabrication technology; Low-temperature techniques

N-channel depletion-mode Si:SiGe modulation-doped field-effect transistors (MODFETs) were investigated in the temperature (T) range between $T = 300$ and 180 K. Operation of Si MOSFETs at low-temperature is known to produce a substantial increase in device performance over room temperature operation [1], mainly through higher carrier mobility and reduced leakage currents. Strained-Si devices on relaxed SiGe virtual substrate (VS) are particularly suited to benefit from cryogenic operation, since the detrimental influence of VS defects on transport properties are reduced at low-temperature, and a better carrier confinement in the Si quantum well can be achieved [2]. The study of cryogenic device operation can also give precious insight in the physical phenomena connected with electronic transport in multilayer heterostructures, since carrier mobilities in the different layers exhibit a different dependence on lattice temperature.

In this work, we present the influence of temperature on the drain current (DC) operation of a Si:SiGe depletion-mode n-MODFET. The layer structure of the device is given in Fig. 1. The (nominally undoped) quantum well channel is separated from the n-doped supply layer (SL) by a 5 nm undoped spacer layer to minimize remote Coulomb scattering. Gate oxide is grown by thermal oxidation at 800 °C to a thickness of ~6 nm. A Si cap layer with a maximum thickness of 4 nm, resulting from incomplete oxidation, may also

* Corresponding author. Tel.: +44-20-7594-6294; fax: +44-20-7594-6308.
E-mail address: v.gaspari@ic.ac.uk (V. Gaspari).

0169-4332/$ – see front matter © 2003 Elsevier B.V. All rights reserved.
doi:10.1016/j.apsusc.2003.08.066

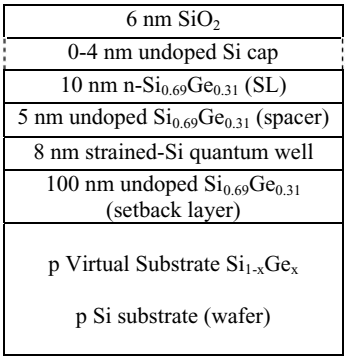

Fig. 1. Layer structure of the device. The Ge content of the virtual substrate is linearly graded from $x = 0$ to 0.31. The supply layer (SL) is As-doped to 10^{18} cm^{-3}.

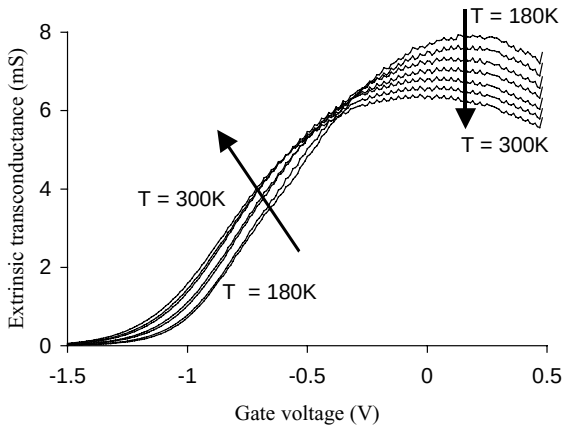

Fig. 2. Measured extrinsic transconductance as a function of gate voltage for $V_{DS} = 1.0$ V and $T = 180$–300 K. The arrows indicate the direction of temperature increase.

be present. The source and drain contacts in Ti/Si were defined self-aligned to the polysilicon gate. The gate length and width are $L = 0.5$ μm and $W = 100$ μm, respectively. Measurements were carried out in a closed-cycle liquid helium cryostat, using computer-controlled Keithleys source-measure units.

The high-field ($V_{DS} = 1.0$ V) transfer characteristics of the device are presented in Fig. 2. As in Si MOSFET devices, the maximum extrinsic transconductance increases monotonically with decreasing temperature, the value at $T = 180$ K being 25% greater than at room temperature. This improvement in transconductance is greater than what is typically reported for submicrometer MOSFETs over the same temperature range [3].

Fig. 3 shows the low-field transfer characteristics of the device ($V_{DS} = 0.1$ V). At room temperature, the transconductance features a broad maximum peaked at a gate voltage of approx. −0.6 V. As temperature is lowered, it appears that such broad transconductance maximum is composed of two peaks, whose relative magnitudes vary with T. A two-peaked transfer characteristic is an indication of the presence of more than one conduction mechanism in the device, such as parallel conduction in the supply layer or, possibly, a second electron channel in the Si cap layer [4]. Indeed, simulations with MEDICI^{TM} show that the influence of conduction through the cap layer to the operation of our device becomes significant if its thickness is greater than 2 nm. The low-field transfer characteristics are quite different from the high-field characteristics, which do not show evidence of parallel conduction. High-field characteristics are probably dominated by conduction in the supply layer, with

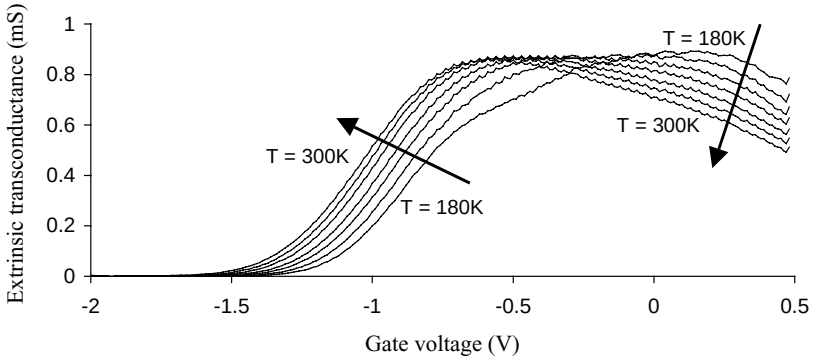

Fig. 3. Measured extrinsic transconductance as a function of gate voltage for $V_{DS} = 0.1$ V and $T = 180$–300 K. The arrows indicate the direction of temperature increase.

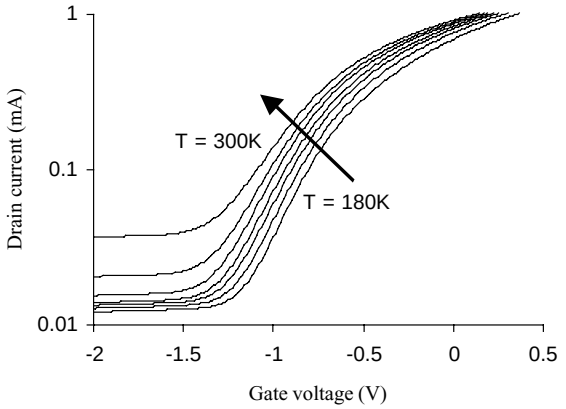

Fig. 4. Measured drain current as a function of gate voltage for $V_{DS} = 0.1$ V and $T = 180$–300 K. The arrow indicates the direction of temperature increase.

mobility suffering a noticeable reduction due to the vertical field.

A low operating temperature also results in a steeper subthreshold slope and reduced off current, as can be seen in Fig. 4. The off current mainly originates from dislocations caused by strain relaxation in the VS, as confirmed by measurements of drain-bulk leakage currents (not shown here). The electrical activity of the energy levels induced by the dislocations is reduced as the temperature is lowered, and as a result the off current is quenched by more than 300% in the investigated temperature range. A summary of device parameters extracted from $T = 300$ to 180 K measurements is given in Table 1.

Table 1
Device parameters extracted from measurements at $T = 300$ K and $T = 180$ K: threshold voltage V_{TH}, field-effect mobility μ_{FE} [6], subthreshold slope S, and contact resistance R_C

T (K)	V_{TH} (V)	S (mV per decade)	μ_{FE} (cm^2/V_s)	R_C (Ω mm)
300	−1.08	640	420	2.6
180	−0.80	430	530	2.1

Two-dimensional simulations have been performed using Synopsys' simulator MEDICI™, in order to qualitatively explain the electrical behavior of the transistor. In the simulations, impurity de-ionization, Fermi–Dirac statistic and mobility degradation due to both longitudinal and transverse electric field have been taken into account. In the study of charge transport in the structure it is of paramount importance to use an accurate modeling of mobility in each layer. Moreover, as temperature decreases the carrier mobility does not exhibit the same dependence on T in each layer as a consequence of different doping levels, alloy scattering in the SiGe layer and lift-off of the valley degeneracy in the strained Si layer. A Monte Carlo model [5] was used to obtain low-field mobilities in strained Si and in bulk $Si_{0.7}Ge_{0.3}$ for each temperature in the studied range and these values were used in the MEDICI™ simulations.

Fig. 5 shows the transfer characteristic of the device, resulting from simulations. Although the simulated behavior does not match the measured transfer

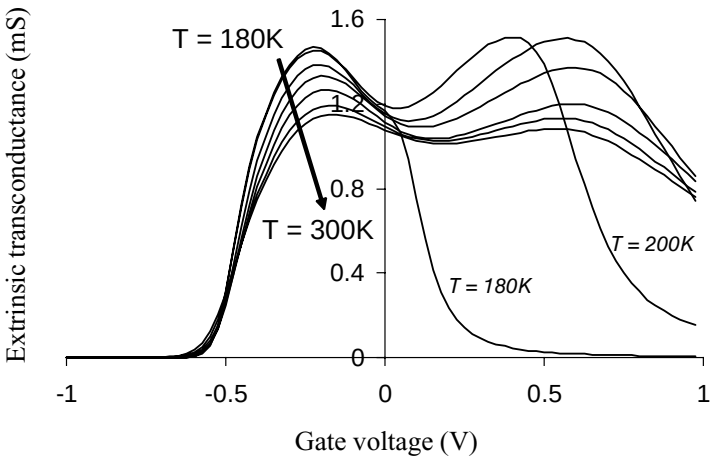

Fig. 5. Extrinsic transconductance as a function of gate voltage for $V_{DS} = 0.1$ V and $T = 180$–300 K as obtained with MEDICI™ simulations.

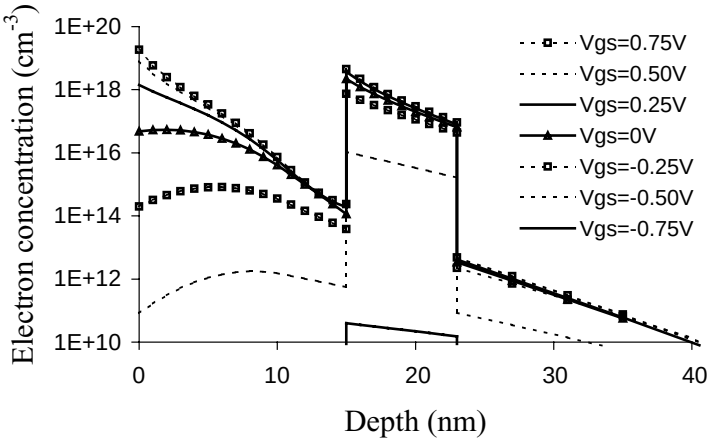

Fig. 6. Electron concentration at the center of the device as a function of the vertical coordinate beneath the oxide, with the gate voltage (V_{GS}) as a parameter, for $T = 300$ K.

characteristic, at this stage of the simulation study (particularly, we can notice the threshold voltage is shifted in simulated characteristics) it is nonetheless significant that the order of magnitude of measured and simulated extrinsic transconductance are the same, and that double peaking can be qualitatively reproduced by simulations. More details on the simulation method can be found in [7].

In order to investigate how a two-peaked transconductance curve relates to the current distribution inside the device, the electron concentration profile was studied for different gate voltages. Fig. 6 shows the electron concentration at the center of the gate as a function of the vertical coordinate beneath the oxide, with the gate voltage (V_{GS}) as a parameter. For low V_{GS} values ($V_{GS} < -0.25$ V, using the gate-to-source voltage values in Fig. 5, that as stated above are shifted by some hundreds of mV in relation to the measured ones), only carriers inside the quantum well channel contribute significantly to the device current, and the sharp increase in their concentration is responsible for the first peak in the transconductance curves. As V_{GS} is further increased, the concentration in the quantum well channel and the spacer layer remains almost unaffected, screened by an increasingly populated supply layer. Indeed, in the $V_{GS} = -0.25$–0.75 V range, the concentration of electrons in the supply layer increases by three to four orders of magnitude, and is the origin of the second peak in the transconductance curves.

In conclusion, the low-temperature operation of a 0.5 μm Si:SiGe depletion-mode n-MODFET was analyzed, with a particular attention to parallel conduction effects, which have been qualitatively reproduced with MEDICI™ simulations.

Acknowledgements

This work was founded by EPSRC through the grant number GR/N65844/01 and by Ministerio de Ciencia y Tecnología (TIC2001-1757) and Consejería de Educación y Ciencia de la Junta de Castilla y León (SA066/02). One of us, JEVP, wish to thank Ministerio de Educación for financial support during his stay at Imperial College under Project Grant PR2002-0175.

References

[1] G. Ghibaudo, F. Balestra, J. Phys. IV 3 (6) (1996) C3-3.
[2] F. Aniel, N. Zerounian, R. Adde, M. Zeuner, T. Hackbarth, U. König, IEEE Trans. Electron. Dev. 47 (7) (2000) 1477.
[3] B. Szelag, F. Balestra, Electron. Lett. 34 (18) (1998) 1793.
[4] U. König, F. Schäffler, Electron. Lett. 27 (16) (1991) 1405.
[5] M.J. Martín, D. Pardo, J.E. Velázquez, J. Appl. Phys. 84 (1998) 5012.
[6] D.K. Schroder, Semiconductor Material and Device Characterization, Wiley/Interscience, New York, 1990, p. 230.
[7] V. Gaspari, K. Fobelets, R. Ferguson, K. Michelakis, S. Despotopoulos, C. Papavassilliou, J.E. Velázquez-Pérez, Thermal study of 0.5 μm-gate Si/SiGe depletion-mode n-MOSFET, in: Proceedings of the Electron Devices Conference, CDE-2003, IEEE Conferences Series, Barcelona, 12–14 February 2003.