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Comparison of sub-micron Si:SiGe heterojunction nFETs to Si nMOSFET in present-day technologies

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Abstract

The measured performance of sub-micron Si:SiGe Schottky gated HFETs is compared to Si nMOSFETs. To allow an up-to-date comparison between Si and strained-Si FETs, the different device types have been studied in their respective technologies. RF performance as given by the cut-off and maximum oscillation frequency is given as a function of input power. The evaluation highlights the current immaturity of the Si:SiGe technologies, where an average HFET shows a maximum transconductance of $\sim$300 mS/mm and cut-off frequency $\sim$60 GHz, while the new generation Si nMOS is reaching 1300 mS/mm and 120 GHz respectively. The comparison shows that the strength of the HFETs lies in low power operation (<200 μW).
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1. Introduction

During the last 10 years, research papers have been published on the possible improvements of SiGe FETs with strained Si channels, both in a buried channel [1,2] and a surface channel configuration [3,4], and compared them to conventional Si nFETs which are traditionally fabricated in the same processing run. Several papers can be found advertising the improved mobility (μ) and transconductance (g_m) [1–4] of strained n-channel Si: SiGe FETs. Virtually no papers can be found on the comparison of the RF characteristics of these different device types. The Si MOS research environment has also been very active, and due to improved processing, record values in both g_{mmax} and cut-off frequency f_T, are reported [5].

Until now, comparisons between SiGe:Si and Si devices are always done with both devices fabricated in the same run within a certain quasi-CMOS compatible process technology. Often these technologies make allowances for the temperature sensitive character of the SiGe material to prevent degradation of the SiGe material system during processing, e.g. reduced processing temperatures are used to avoid substantial Ge segregation [6]. Although this type of comparison is extremely useful to establish performance improvements to an in-house benchmark, they do not represent the current state-of-the-art Si MOS performance. To allow a more commercially sensible comparison of where both technologies (Si versus SiGe:Si) stand at the moment, each device type has to be processed in its own technology.

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Table 1
Measured record values in three FET technologies, maximum transconductance, g_{mmax}, cut-off frequency, f_T, and maximum oscillation frequency, f_{max} (both de-embedded)

	g_{mmax} (mS/mm)	f_T (GHz)	f_{max} (GHz)	Reference
HFET	570	90	107	[1,2]
Strained-Si MOSFET	340	NA	NA	[3]
Si MOSFET	1100	150	80	[5]

HFET is a Schottky gated strained Si buried channel FET, the strained-Si MOSFET is a MOS gated surface channel FET, the Si MOSFET is multiple metal gate-finger MOSFET with elevated source and drain.

The current values for the different device types in their respective technologies, taken from published literature, are given in Table 1.

No MOS-gated Si:SiGe buried channel (BC) FETs have been reported to have f_T in the same range [7]. RF measurements done in-house on MOS-gated Si:SiGe buried channel FETs give only $f_T = 500$ MHz embedded on 1 μm gate length devices, while measurements on 0.5 μm gate length strained-Si MOSFET give embedded f_T of 720 MHz and the Si MOSFET processed in the same run $f_T = 800$ MHz embedded. Due to a lack of suitable de-embedment structures, no de-embedded values could be generated. The results though illustrate poor BC MOSFET performance and higher parasitics in the strained-Si devices as the DC performance was found to be better than the Si control in these wafers.

In this paper we present a comparison between Schottky-gated HFETs designed, grown and processed by the research group in Daimler–Chrysler and Si MOSFETs designed and processed by IMEC. Both devices are designed for high frequency operation. The RF comparison is made at both low and full power.

All measurements are done using a 50 GHz Agilent 8510C network analyser controlled by Agilent ICCAP software.

The paper is organised as follows, in Section 2 we discuss the measurement requirements for low power RF measurements and we show the impact of a failure to adhere to these requirements. In Section 3 we describe briefly the device geometries, Section 4 gives the RF comparison between the Si and SiGe:Si devices. Conclusions can be found in Section 5.

2. Measurement requirements

In low power RF measurements the input power on the gate has to be sufficiently low to allow for the small signal equivalent model, relying on a linearisation of the characteristics around the bias point, to be valid.

In sub-threshold the DC current–voltage characteristic of a FET follows an exponential characteristics and is given by [8]:

$$I_d = \frac{\mu W (C_d + C_{it}) V_T^2}{L} \exp\left((V_{GS} - V_{th})/V_T \times \left(1 + \frac{(C_d + C_{it})}{C_i}\right)^{-1} \right) \left(1 - \exp\left(\frac{V_{DS}}{V_T}\right)\right) \quad (1)$$

with μ mobility, L and W gate length and width respectively, C_d diffusion capacitance, C_{it} interface state density capacitance, C_i gate insulator capacitance, V_T thermal voltage, V_{th} the threshold voltage, V_{GS} and V_{DS} the gate and drain voltage respectively, referred to the source.

When an AC gate voltage $v_{G_{ac}}$ is added to the DC biasing point, (1) becomes:

$$I_d = I_0 \exp\left(\frac{nV_{G_{DC}} + v_{G_{ac}}}{V_T}\right) \quad (2)$$

with n and I_0 constants related to the parameters given in (1) and V_{DS}.

As the bias point is applied via voltage divider action and not by rectification of the RF drive, the input power defines a Thevenin source of 50 Ω, and a voltage amplitude given by Eq. (3) for input power P_G.

The upper limit of the input power (P_G) on the gate into a 50 Ω load, is given by:

$$P_G = \frac{1}{2}\frac{v_G^2}{50} \quad \text{or} \quad v_G = 1010^{\frac{P_G\ (\mathrm{dBm})}{20}} \quad (3)$$

with v_G the peak voltage and P_G given in dB m. The percentage variation on DC current is expressed as:

$$I_{tot} = I_{DC} + V(\%)I_{DC}$$

The varying gate voltage and percentage variation versus power input relation is given in Fig. 1.

This result shows that the input power needs to be sufficiently small to avoid non-linear variation of the source–drain current around the DC biasing point.

The actual gate drive voltage is guaranteed to be less than that of Fig. 1, since a voltage divider is set up between the source and the gate.

In Fig. 2 we illustrate the influence of the gate input power on the extracted de-embedded values of the cut-off frequency. Measurements are presented at V_{GS} slightly above threshold for low V_{DS} as maximum low

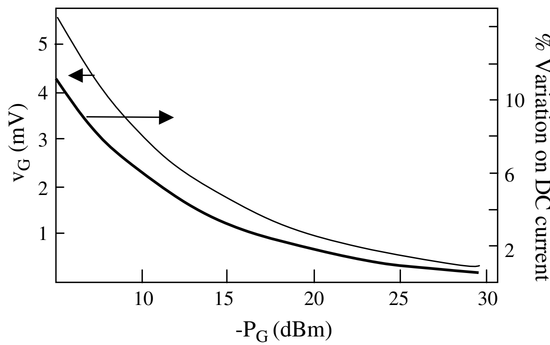

Fig. 1. Peak value of the varying gate voltage as function of the input power on the gate expressed in dB m. Percentage variation V(%) on the DC current as a function of gate input power. The values for P_G are negative.

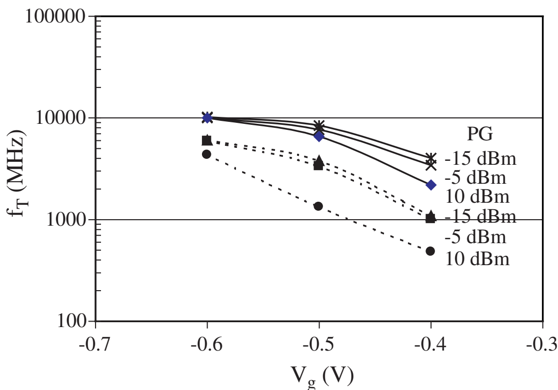

Fig. 2. Cut-off frequency as a function of gate voltage, for two drain voltage values: full lines: $V_{DS} = 0.1$ V, dashed lines: $V_{DS} = 0.05$ V, and varying gate input power P_G: −15, −5 and 10 dB m.

power performance occurs in this region [9]. It is worthwhile to note that the concept of saturation is not as characteristic in weak inversion as it is in strong inversion. Indeed, a few kT suffice for weak inversion saturation. Moreover the performance maximum in these devices is very close to the boundary between triode and saturation.

As can be seen in Fig. 2, too high input power values, result in reduced cut-off frequency readings. In this work we have taken −15 dB m gate input power as a compromise between the lower noise level and the linearity of the device characteristics around the biasing point.

3. Brief description of the RF transistors

The n-channel HFET structures presented in this paper are grown by MBE on an LEPECVD virtual substrate (VS) graded up to 40% Ge grown on a high resistivity p-type substrate. The layer structure from bottom to top is: VS, constant composition $Si_{0.6}Ge_{0.4}$ layer, 5 nm Sb doped $Si_{0.6}Ge_{0.4}$, 5 nm undoped $Si_{0.6}Ge_{0.4}$, 9 nm Si strained channel, 3.5 nm undoped $Si_{0.6}Ge_{0.4}$, 5 nm Sb doped $Si_{0.6}Ge_{0.4}$, 3.5 nm Si cap layer. HEMT compatible processing was performed with added ohmic contact P doping implantations followed by low thermal anneal and deposited SiO_2 passivation. The ohmic contact metal is Ti/Pt/Au and the recessed e-beam written Schottky gate is Pt/Au. The devices measured for the comparison have a gate length, L_g of 0.1 μm and gate width of 100 μm, the distance between source and drain contacts is 1 μm. The sheet resistivity of the layers is 811 Ω/□, the sheet electron density is $n_s = 4.5 \times 10^{12}$ cm^{-2} and the corresponding Hall mobility is 1700 cm^2/V s (all at 300 K). Ohmic contact resistance is 30 Ω for both source and drain contacts.

The n-channel Si MOSFET is designed for LNA (low noise applications) and is defined on p-type high resistivity wafer, using shallow trench isolation, well doping and consisting of a thin 1.5 nm gate insulator. The gate is 150 nm thick pre-doped silicided polySi with a low contact resistance of 7 Ω□. Salicided source/drain contacts are used. Full details of the process can be found in [5]. The devices measured in this work have two-fingered gates with 20 μm finger width each and 0.1 μm gate length.

4. RF comparison between Si nMOS and buried channel Si:SiGe n-HFETs

The Si MOSFET performance is very homogeneous across the wafer as a result of the tight processing control. The variation of the HFET performance across the wafer is a result of the in-homogeneities mainly in the growth of the device layers and in the processing. For the comparison not the best device but a device with average performance across the wafer was chosen. As voltage and current levels where optimal performance is reached in both device types differ, the RF performance data is given as a function of DC bias input power $P = I_{DS}V_{DS}$. V_{DS} was limited to 1.2 V and gate overdrive voltage $V_{GS} - V_T$ was limited to 0.7 V. The intrinsic cut-off frequency f_T and the maximum oscillation frequency f_{max} of both devices are measured at low gate ac input powers (−15 dB m).

The cut-off frequency f_T as a function of input bias power P is given in Fig. 3. The graph shows maximum f_T for the minimum applied power. This corresponds to bias settings at maximum transconductance, which falls in the region between triode and saturation in these devices. It is obvious that although the SiGe HFETs perform quite well (measured f_T lower than reported maximum values [1]), the new generation Si nMOS, based on well-explored CMOS technology and including

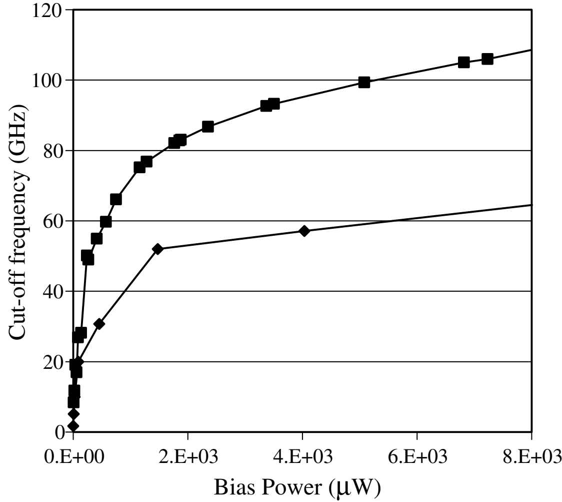

Fig. 3. The de-embedded maximum cut-off frequency f_T versus minimum bias power P for both Si (squares) and SiGe (diamonds) over a wide bias power range. Bias points correspond to the point of maximum transconductance and lie for both devices in the region between triode and saturation.

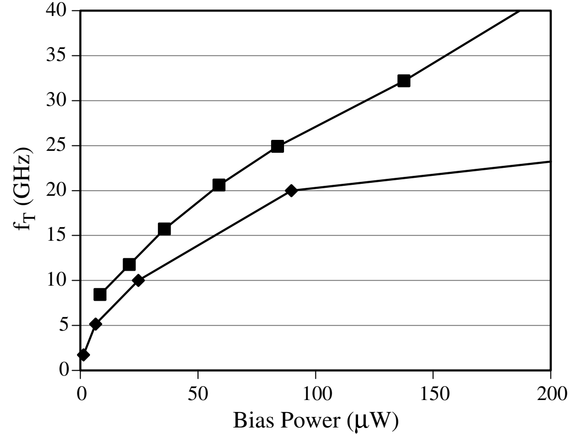

Fig. 4. Low power performance of the Si nMOS (squares) and the SiGe:Si HFET (diamonds). Bias points correspond to the maximum transconductance.

the most recent processing developments, show almost twice the cut-off frequency compared to the SiGe devices (measured f_T in close agreement with [5]). The main reason for this is the still immature SiGe processing technology, low thermal anneal and the large source-gate and drain-gate distances imposed by the current processing rules, which result in large contact resistances R_s and R_d. As can be seen from equation (4), high source and drain resistance R_s and R_d will lower g_m and f_T.

$$f_T = \frac{g_m}{2\pi\left[(C_{gs} + C_{gd})\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + g_m C_{gd}(R_s + R_d)\right]} \tag{4}$$

In (4), R_{ds} is the differential channel output resistance, C_{gs} and C_{gd} are respectively the gate-source and gate-drain capacitances. Interestingly, when focussing on the low power region $P < 100$ μW (see Fig. 4), one notices that both curves are almost converging. At low power the immature SiGe technology shows equivalent performance to the Si device. Similar behaviour has been seen on better performing HFETs [9]. This demonstrates SiGe HFETs' potential for low power applications (at low V_{DS} and low gate voltage overdrive as illustrated in [9]) when compared to Si nMOS. This performance enhancement of buried channel devices at low power was already suggested in DC measurements by Welser et al. [10].

The main requirements for good low power operation of the SiGe devices is low leakage currents. The dislocation density near the pn junction isolation between device and substrate must be kept low to avoid parallel conduction via the substrate layers. To avoid parallel conduction through the supply layers and to optimise the transconductance the top supply layer needs to be sufficiently thin but allowing Schottky gating and the bottom supply layer needs to be removed for low power operation. These requirements guarantee that the majority of carriers travel in the high mobility strained Si buried channel. In this respect the HFET layer structure as used in this study can be further optimised for low power operation [11].

The maximum oscillation frequency reached in these devices shows that the gate resistance R_g is the main player in the performance, as given in Eq. (5).

$$f_{max} = \frac{f_T}{2\left[\left(\frac{R_g + R_s + R_i}{R_{ds}}\right) + 2\pi f_T R_g C_{gd}\right]} \tag{5}$$

The performance comparison between HFET and nFET is given in Fig. 5. We notice that the maximum oscillation frequency f_{max} in our HFET is reaching a record value of 113 GHz, which is far above the value for the double gate finger nMOS. This is not surprising as although the nMOS was fabricated for LNA, the gate resistance R_g of the metal Schottky gate is dramatically smaller than the silicided in situ doped polySi gate. Increasing the amount of parallel gate fingers to 5 will improve f_{max} by a factor of 2.5 compared to the used nMOS.

The low power performance of the HFET, however better, is very close to that of the nMOS. The behaviour of both devices at very low input power is given in Fig. 6 as a function of gate overdrive. Although the HFET still delivers the highest value for f_{max} in a certain gate overdrive range, the performance variation is completely

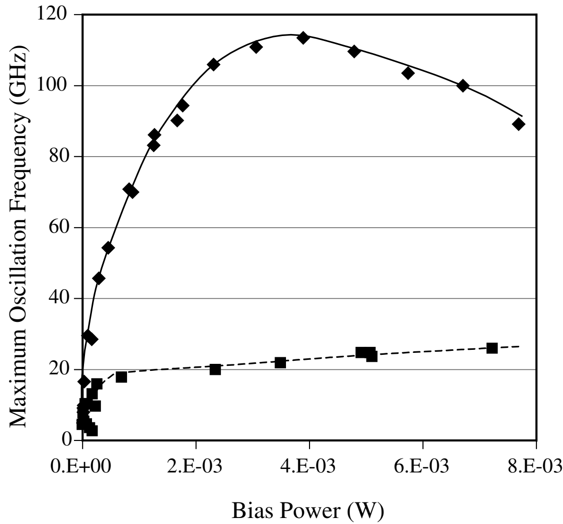

Fig. 5. The maximum oscillation frequency f_{max} versus minimum bias power for the Si nMOS (squares) and the SiGe:Si HFET (diamonds). Bias points correspond to the maximum transconductance.

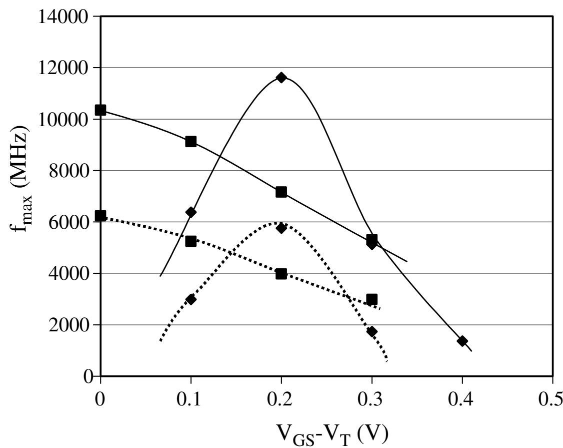

Fig. 6. The maximum oscillation frequency versus gate overdrive for the Si nMOS (squares) and the SiGe:Si HFET (diamonds). Plain lines are for $V_{DS} = 0.01$ V and dashed lines for $V_{DS} = 0.06$ V.

different from the nMOS. The peaked characteristic of f_{max} for the HFET as a function of gate overdrive is in contrast to the monolithic variation of f_{max} for the nMOS. Looking at Eq. (5) we notice that apart from extrinsic parasitics, f_{max} is strongly correlated to the intrinsic factor $R_{int} = R_i/R_{ds}$—the ratio of the differential channel input resistance R_i to the differential channel output resistance R_{ds}. R_{int} is calculated from the differential resistances derived from the DC characteristics of the device as $R_i = (\frac{dV_{GS}}{dI_{DS}})$ to first order and $R_{ds} = (\frac{dV_{DS}}{dI_{DS}}) - R_s - R_d$. R_s and R_d for the HFET are derived from both

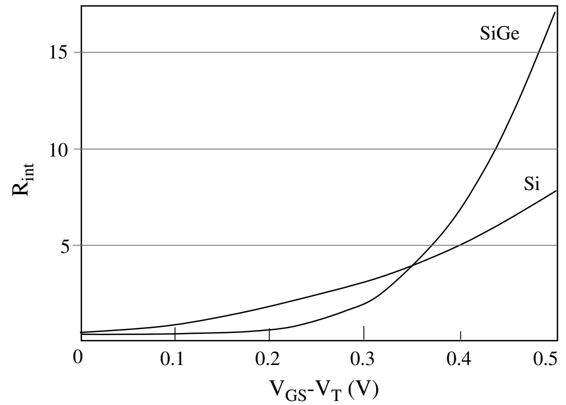

Fig. 7. The variation of the ratio of the differential channel input resistance to the differential channel output resistance as a function of gate voltage overdrive for $V_{DS} = 0.06$ V.

DC and RF measurements [12], while the source and drain resistance in the nMOS is neglected compared to the channel resistance. Fig. 7 shows the variation of R_{int} as a function of gate overdrive. We observe that this ratio is lower in the HFET than the nMOS up to a certain level of gate overdrive when R_{int} increases suddenly at 0.4 V gate overdrive for the HFET, causing the drop in f_{max}. Notice the non-linear variation of R_{int} for the HFETs. This non-linearity becomes more pronounced at higher V_{DS} values. We suggest that the non-linear variation of R_{int} is correlated with the peaking of the maximum oscillation frequency f_{max} curve for the HFET. In contrast, R_{int} for the nMOS increases monolithically causing a monolithic decrease of f_{max}.

5. Conclusions

The Si nMOS outperforms the average SiGe:Si HFET on current gain performance: 130 GHz versus 60 GHz cut-off frequency. This is mainly attributed to high contact and access resistances in the HFET device collated to processing issues. The low power performance of the HFET though is already very similar to that of the Si nMOS, indicating a promising application area for the HFETs for the near future. Some strategic layer structure changes have to be made for optimal low power performance in HFETs.

The low gate contact resistance R_g of the HFET Schottky gate ensures that the HFET outperforms the nMOS on maximum oscillation frequency, f_{max}. A record value is recorded of $f_{max} = 113$ GHz. The variation of the maximum oscillation frequency of the HFET peaks at small gate overdrive while for the nMOS, f_{max} decreases monolithically, which is a result of the variation of the ratio of the input to output resistance of the channel.

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