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Buried-channel SiGe HMODFET device potential for micropower applications

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Abstract

In this paper, intrinsic device parameters, directly extracted from buried-channel n-HMODFET devices biased at micropower supply levels are presented. Sub-threshold region peaks in plots of intrinsic transit frequency and transconductance vs. bias clearly exemplify the devices suitability for RF/micropower applications. Measurements are also presented for a SiGe n-HMODFET inverting amplifier and self-biased dynamic load with a maximum (G_{MAX}) power gain of 26 dB and corner frequency of 40 MHz recorded for an amplifier device power-drain of just 77 μW and a total power drain of 150 μW. A comparison of gain-efficiency (maximum gain vs. total input power) at micropower (200 mV V_{DD}) and full power (3 V V_{DD}) yields 4× greater efficiency at micropower supply levels.

Keywords: SiGe; HFET; Micropower; Low-voltage; Parameter extraction

1. Introduction

SiGe HMODFET device research is driven by the need to improve the high-frequency and low-power performance of the Si MOSFET whilst retaining compatibility with well-established Si CMOS processing [1]. In strained buried-channel HFET devices, a heterojunction is created in the device by forming a channel using a thin high-mobility strained Si n-type layer and separating this from the gate by the addition of further p-type SiGe semiconductor 'buffer' layers [2–6]. The most salient feature of these devices is that they exhibit an extra boost in transconductance (g_m) at low bias levels when compared to conventional MOSFETs due to a lower sub-threshold slope at high V_T, the higher mobility offered by the strained Si channel and the removal of carriers from the SiO_2 interface [4,7]. Recently in [8] an n-type Si/SiGe strained channel device's mobility was reported to be 30% more than that of a MOSFET. RF micropower (μ_p) capable devices such as these are clearly suited to applications in which battery life and/or overall heat dissipation are an issue [9].

In analogue design, low power operation usually means the use of low voltage supply, because power is a function of applied voltage and drawn current [10]. The absolute limit to low power operation in analogue circuits is set by the requirement to maintain the signal energy at a higher level than that of thermal energy, in

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order to keep the signal to noise ratio, S/N, at a practical level. Hence, the minimum power required is a function of S/N, $P_{min} = 8fkTS/N$ [11], where f is the measured signal bandwidth. In practice, it is difficult to achieve the required S/N at micropower levels because power is proportional to S/N and frequency [11]. FETs biased into sub-threshold operation have traditionally been used for micropower design as the current response within this region, being exponential in nature, is similar to that of bipolar junction transistors, with the transconductance, g_m, being the maximum achievable for a given value of drain current even though I_{DS} is invariably low [12,13].

A very low noise figure of 0.3 dB [14], has been reported for these strained buried channel devices and this fact, together with their acknowledged higher-than-MOSFET channel carrier mobilities at low V_{DS}, qualifies them for use in micropower circuit design. However, there is to date, no published data on the use of these devices in RF circuits operating at micropower levels (sub 1 mW) with the exception of [15] in which the authors demonstrate the use of one of these devices in an RF micropower amplifier using an integrated resistive load and 0.5 μm gate-length by 100 μm gate-width device as the active driver.

In this work we will show that sub-threshold region peaks in both the transconductance and transit frequency of these devices, attributable to the higher mobility of the carriers confined to the strained channel at low V_{DS} and to the reduction of surface roughness scattering due to the surface to channel separation offered by the use of a buried channel, attest clearly to their micropower potential.

We present intrinsic device gain behaviour, directly extracted from DailmlerChrysler fabricated devices at micropower supply levels, that supports the suitability of these devices for RF/micropower applications. We also present, for the first time, a fabricated all n-type device micropower amplifier in which the active load is made from a self-biased n-HMODFET device of 0.25 μm gate-width and 30 μm gate-length. The device structure and fabrication method are given in [15], the extracted intrinsic device micropower gain behaviour is presented in Section 2, the amplifier's measured ac characteristics are compared for both micropower and full-power levels in Section 3 and we conclude in Section 4.

2. Intrinsic device gain behaviour

Active FETs with 0.1 μm gate-lengths and 100 μm gate-widths, as well as open and short devices were probed on-wafer. S-parameter measurements were made using a HP5783D Network Analyser, DC I_{DS} for each bias point was recorded automatically using a programmed system of Keithley sources and the two-step de-embedment procedure given in [16] was applied to de-embed pad parasitics. The devices have been experimentally assessed to have a safe maximum V_{DS} range of +1.5 V before breakdown becomes likely.

The pinch-off voltage extracted from a fabricated 'T' gate device's DC–IV characteristics is illustrated in Fig. 1. An experimental approach using 1% of I_{DSS} [17], resulting in an extracted pinch-off voltage, V_p, of −0.7 V, is used here because these devices do not follow the square-law characteristic typical of inversion layer MOSFETs operating in the saturation region and hence the commonly used extrapolation from a plot of $\sqrt{I_{DS}}$ vs. V_{GS} is not applicable. The graph also illustrates the fact that the present devices suffer from unusually high levels of pinched-off leakage current (~300 μA). The

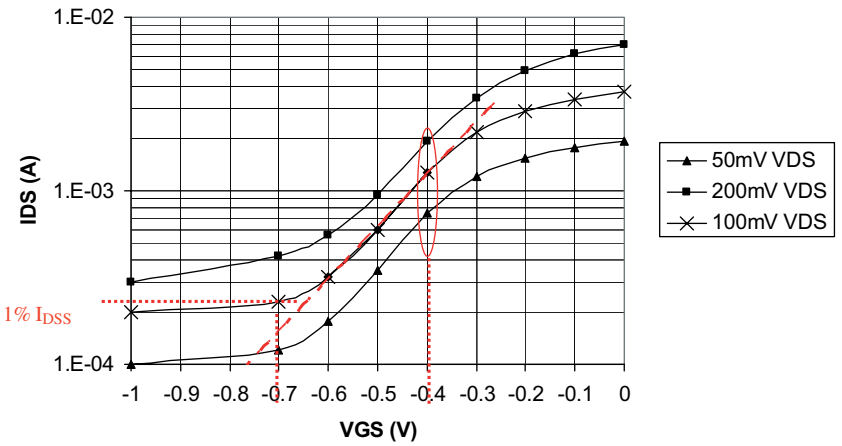

Fig. 1. Pinch-off voltage extraction from input DC–IV characteristics. A V_p of −0.7 V is extracted by taking the point at which $I_{DS} = 1\%$ of I_{DSS} for 0.1 V V_{DS}.

points around −0.4 V V_{GS} are circled in Fig. 1 to emphasise that this bias zone encompasses the transition between the sub-threshold and linear regions of operation. This bias zone is of special importance as the following intrinsic parameter extractions will show that device performance is enhanced within this zone.

The intrinsic transit frequency, f_T at each bias point was extracted by noting the point at which the plot of $|H_{21}|^2$ intercepts the frequency axis, an example is shown in Fig. 2, and these were plotted vs. total power drawn in Fig. 3 and vs. bias in Fig. 4. f_T's of 10 GHz at 30 μW and 30 GHz at 400 W give a good indication of the RF capability of these devices at micropower supply levels. Also, a consistent peak in f_T at around −0.4 V V_{GS} for low V_{DS} is illustrated by Fig. 4, although this peak tends to manifest at higher V_{GS} bias as V_{DS} is increased.

The intrinsic transconductance, g_m, is extracted using the real part of intrinsic Y_{21} as given by $g_m \approx Re(Y21_i)|_{\omega\to 0}$ and is plotted vs. bias in Fig. 5 with a peak in g_m, at around −0.4 V V_{GS} for low V_{DS}, clearly evident. Also worthy of note is that there is little increase in g_m (+25%) between 200 mV V_{DS} (18 mS) and 1 V V_{DS} (24 mS) at −0.3 V V_{GS} compared to the +500% increment between 10 mV V_{DS} (1 mS) and 50 mV V_{DS} (5 mS) at −0.4 V V_{GS} and this further emphasises the micropower suitability of these devices.

The total output resistance, or inverse of the total output conductance, is composed of the ohmic drain contact, RD, the ohmic source contact, RS, and the intrinsic channel resistance, r_{ds}. The expression used to obtain the total output conductance is given by $g_{ds} \approx Re(Y22_i)|_{\omega\to 0}$. DaimlerChrysler process data states

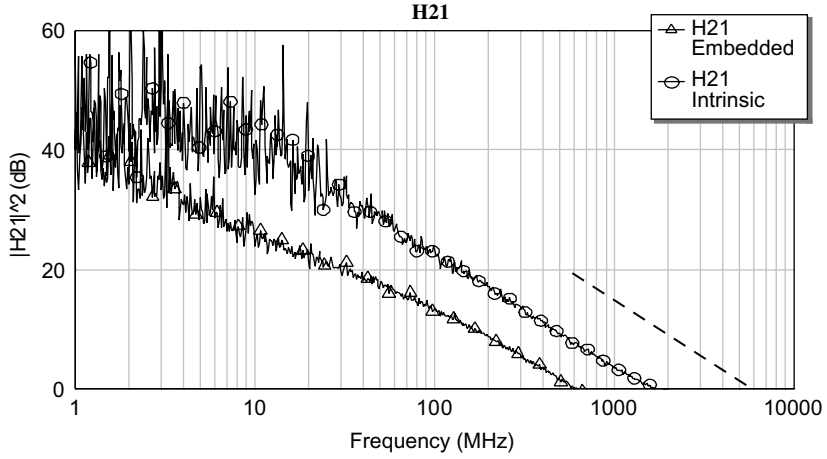

Fig. 2. Transit frequency extraction from $|H21|^2$. An f_{ti} of 1.8 GHz at 0 V V_{GS} and 50 mV V_{DS} is shown.

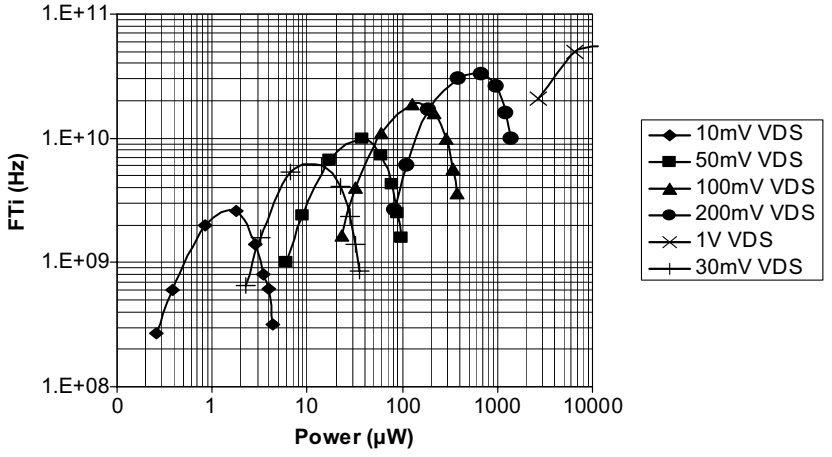

Fig. 3. Intrinsic transit frequency vs. power drain. F_T's of 10 GHz at 30 μW and 30 GHz at 400 μW can be noted.

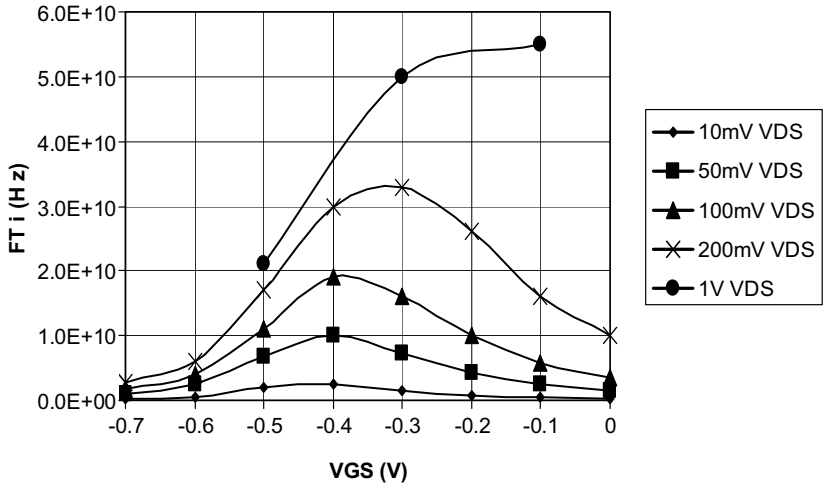

Fig. 4. Intrinsic transit frequency vs. bias. A peak in f_T around −0.4 V V_{GS} at low V_{DS} is illustrated.

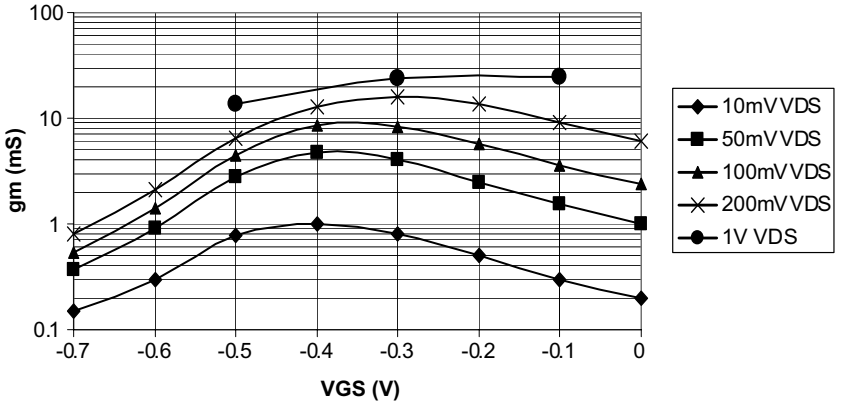

Fig. 5. Intrinsic transconductance vs. bias. Transconductance peaks at around −0.4 V V_{GS} for low V_{DS}.

an approximate value of 3 Ω mm for ohmic resistances and this translates to RD = RS = 30 Ω for a 100 μm wide device, giving a total ohmic contact resistance of around 60 Ω. In operation, the extracted channel resistance will approach the total value of contact resistance as the device leaves the linear region of operation and begins to operate within the sub-threshold region. This fact is illustrated by the chart of extracted total channel resistance vs. bias, shown in Fig. 6, where the total channel resistance is seen to approach the combined value of RD and RS (60 Ω) for $V_{GS} < -0.4$ V and $V_{DS} < 100$ mV, thus severely limiting the intrinsic output voltage swing. This, in turn, results in an intrinsic voltage gain of less than unity below 100 mV V_{DS}. Intrinsic voltage gain is obtained from expression (1) and is illustrated in Fig. 7, wherein a maximum A_V of 12× is evident at 1.5 V V_{DS}.

$$A_V \cong -\frac{Y21_i}{Y22_i} \tag{1}$$

Thus, the relatively high values of ohmic contact resistances RD and RS become a limiting factor in the usefulness of these devices for operation at very low voltage supply levels ($V_{DS} < 100$ mV) and it is expected that micropower performance at these voltage supply levels will improve if these contact resistances are reduced, for example, by the use of heavier doping and the introduction of self-aligned gate techniques that reduce the source to gate distance. In the present devices, the distance from source and drain to the gate is 0.45 μm and the gates are not self-aligned.

3. Amplifier measurement and comparison

The fabricated amplifier measuring 44 μm × 300 μm, Fig. 8, was probed on-wafer using a HP5783D Network Analyser. DC bias was supplied to the gate of the driving device via the analyser's built-in DC 'T' bias

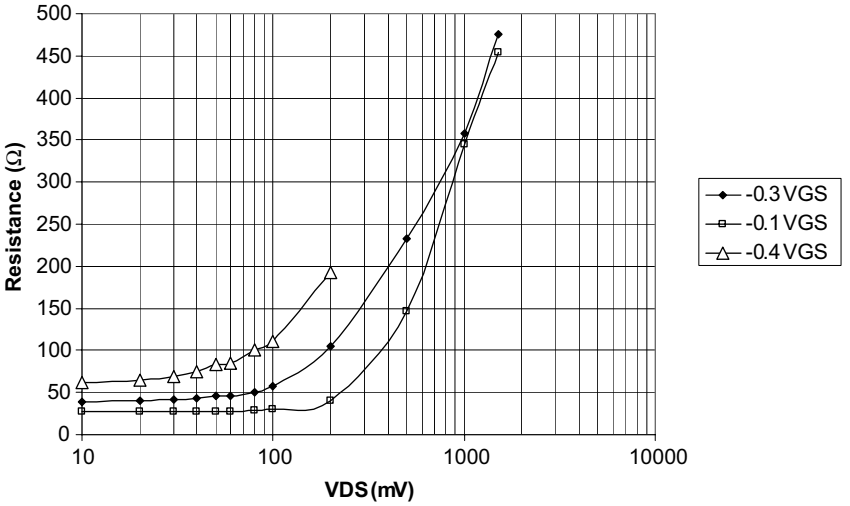

Fig. 6. Total channel resistance vs. bias. There is little change in resistance vs. V_{DS} for $V_{DS} < 100$ mV indicating the dominance of the drain and source ohmic contact resistance below this bias level.

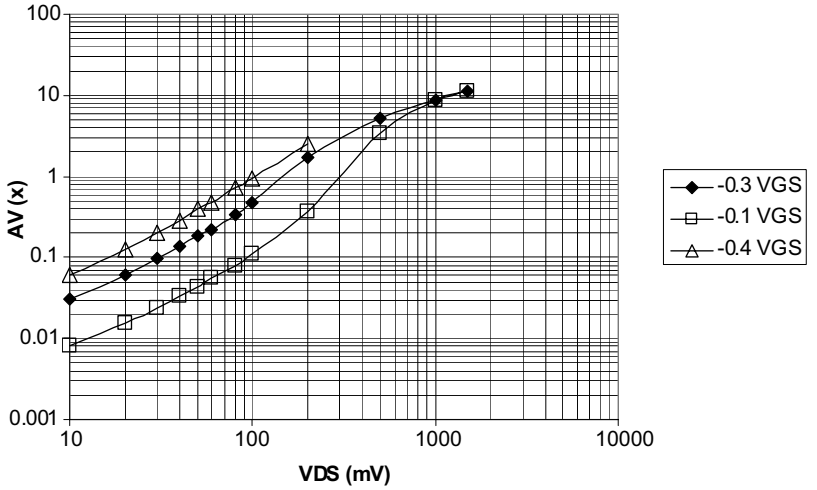

Fig. 7. Intrinsic voltage gain vs. bias. $A_V < 1$ for $V_{DS} < 100$ mV and $A_V = 12$ @ 1.5 V V_{DS}.

connector in Port 1; Port 2 was connected to the junction of both FETs and a DC supply was also connected to the load device's drain.

The drain current and the voltage across each device vs. gate bias were automatically recorded by a pair of Keithley sources and these are plotted vs. power-drain in the driving device, Figs. 9 and 10, where the peak in drawn power, 77 μW @ 200 mV V_{DD} and 9.2 mW @ 3 V V_{DD}, are shown occurring very close to the optimum mid-bias points (−0.33 V V_{GS}) on both charts. S-parameter data was then recorded for a range of V_{GS} values using an input power of −25 dBm to avoid gate-overdrive and this data was used in MWOffice Software [18] to extract the amplifier's maximum power gain (G_{MAX}-2), corner-frequency and unit-gain bandwidth vs. gate-bias for both supply conditions, μ_p @ 200 mV V_{DD} and F_p @ 3 V V_{DD}, Fig. 11.

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|}(k - \sqrt{k^2 - 1}) \tag{2}$$

where

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}||S_{21}|} \tag{3}$$

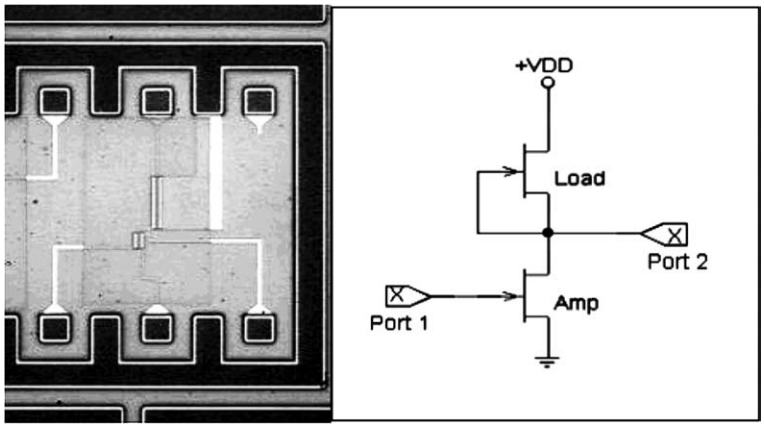

Fig. 8. Photomicrograph of inverting amplifier and equivalent circuit.

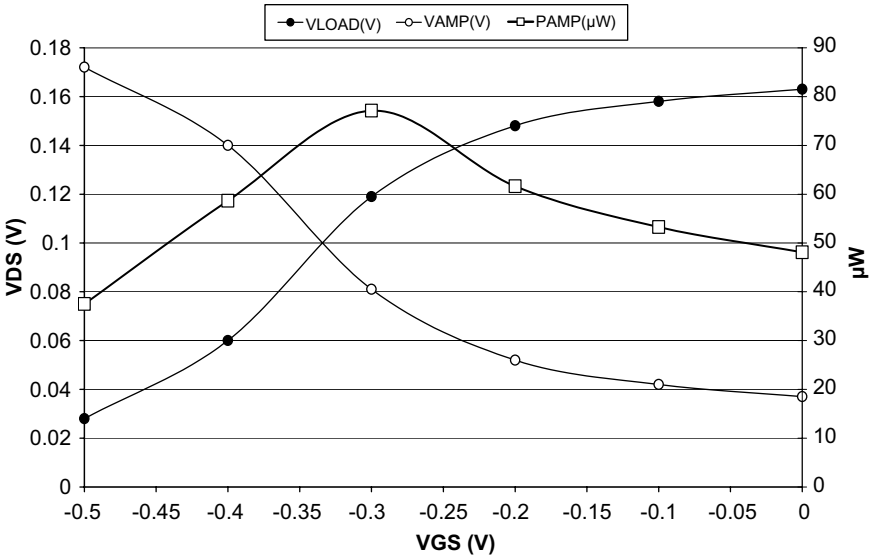

Fig. 9. Device DC potentials and amplifier power drain vs. V_{GS} at 200 mV V_{DD}.

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4}$$

Fig. 11 shows a corner frequency of 40 MHz at −0.33 V V_{GS} for a total power drain of 150 μW and a F_p −3dB bandwidth of 6.2 MHz is also shown. These bandwidths would improve further with the use of RF matching techniques as the measured unit gain-bandwidths at both supply levels are in excess of 7 GHz.

A maximum power gain of 26 dB at a total power-drain of 150 μW and a power-gain of 40 dB at a drain of 15 mW can be gleaned from Fig. 12. For the purpose of comparison, these two peak gains can be scaled and evaluated and we then find that μ_p efficiency is 4× that of F_p efficiency:

$$\mu_p \text{ gain} = 26 \text{ dB} = 398 \times @ 200 \text{ mV} \quad \text{with 150 μW power-drain} \tag{5}$$

$$F_p \text{ gain} = 40 \text{ dB} = 10000 \times @ 3 \text{ V} \quad \text{with 15 mW power-drain} \tag{6}$$

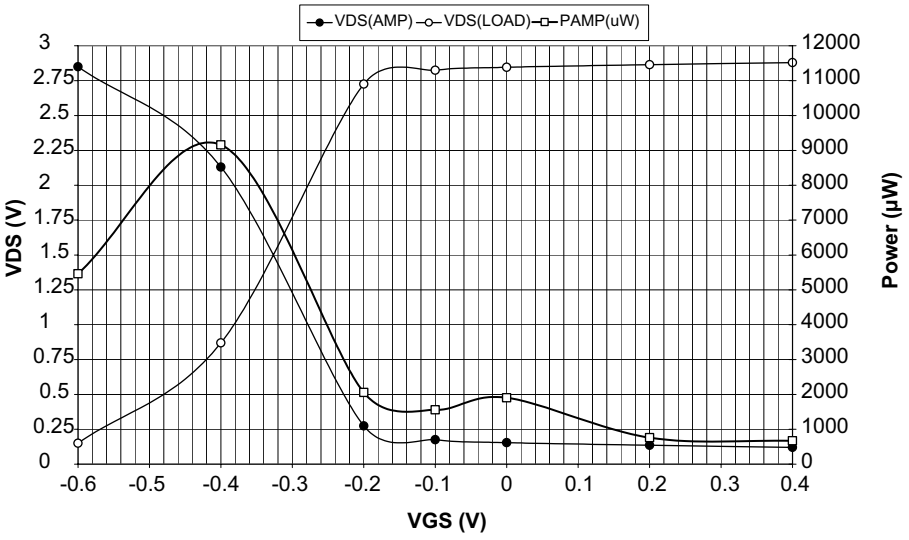

Fig. 10. Device DC potentials and amplifier power drain vs. V_{GS} at 3 V V_{DD}.

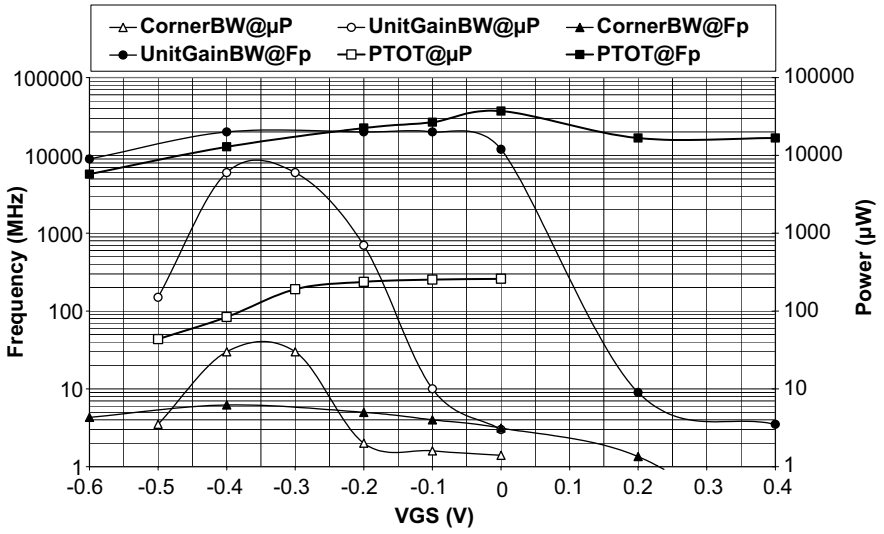

Fig. 11. Bandwidth and total power drain vs. V_{GS} at 200 mV and at 3 V V_{DD}.

Dividing the F_p gain, (6), by the power-drain advantage:

$$40\ \text{dB} \div \left(\frac{15 \times 10^{-3}}{150 \times 10^{-6}}\right) = 20\ \text{dB} \tag{7}$$

Dividing μ_p gain, (5), by the normalised F_p gain, (7):

$$26\ \text{dB} - 20\ \text{dB} = 6\ \text{dB} = 4\times \tag{8}$$

It can also be noted from Fig. 13 that the equivalent resistance of the load device at $F_p(\sim 300\ \Omega)$ is more than twice that at $\mu_p(\sim 130\ \Omega)$ and hence even though the larger value of R_L increases the gain of the circuit at F_p we find that the amplifier is still many times more efficient at μ_p supply levels.

4. Conclusion

The extracted intrinsic gain behaviour of buried-channel n-HMODFET devices has been presented. The 100 nm gate length devices have a measured f_t of 30 GHz at 200 mV V_{DS} and at 400 µW total power drain.

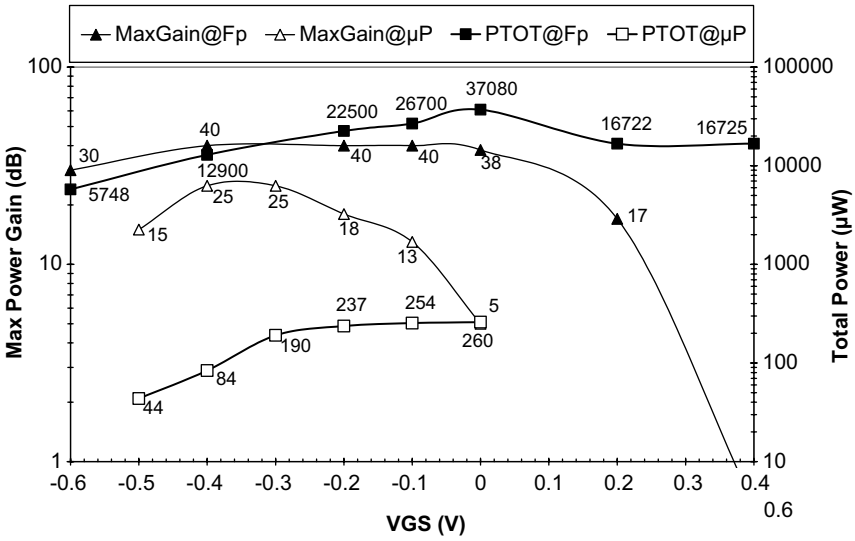

Fig. 12. Maximum gain and total power drain vs. V_{GS} at 200 mV and 3 V V_{DD}.

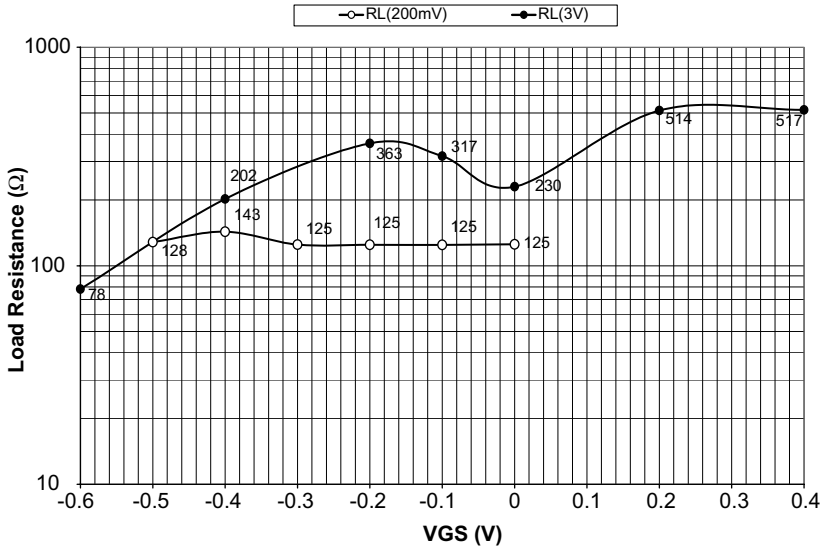

Fig. 13. Load resistance vs. V_{GS}.

Despite fairly high leakage current exhibited when pinched-off, their suitability for RF/micropower applications is asserted by consistent sub-threshold region peaks in transit frequency and transconductance at low V_{DS} bias but it is noted that device voltage gain and hence micropower performance at very low V_{DS} (sub 100 mV) is hindered by ohmic contact resistances RD and RS as output signal is lost to these. Unless these are significantly reduced, the relatively low voltage gain resulting as a consequence means that circuit applications would need greater care in the design phase and that different approaches may need to be adopted, e.g. the use of impedance matching techniques to maximise power transfer at RF frequencies or the employment of a current-mode topology as suggested in [19], which is suited to the low output resistance exhibited by these short channel devices and is more appropriate to exploiting their current gain at low V_{DS}.

A realised all n-type depletion-mode SiGe HMODFET based, micropower capable RF amplifier using a self-biased n-type device as load has also been presented here for the first time. Measured results of power-gain and bandwidth vs. gate-bias show the amplifier to have a maximum gain of 26 dB at a total power-drain of 150 μW, with a unit-gain bandwidth of 8 GHz and corresponding half-power bandwidth of 40 MHz. A com-

parison of the amplifier's gain-efficiency at micropower (200 mV V_{DD}) and at full power (3 V V_{DD}) gives an improvement of 4× at micropower supply.

The circuit results presented also confirm that these devices are more efficient at low voltage/micropower operation than when operated at full power and hence, it should be clear from all the results presented here, that the most sensible way forward with this technology is to minimise channel lengths to the point where suitable transit frequencies are achieved (we are of the opinion that L should be $\leqslant 100$ nm), to drastically reduce access resistance and render its effect on voltage gain minimal and to adopt alternative circuit design topologies which are better suited to the exploitation of the benefits inherent to these devices.

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