



Current Mode, Voltage Mode, or Free Mode? A Few Sage Suggestions

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Abstract. Many claims have been made about the benefits of a *current-mode* (CM) approach to IC design. The term is used to draw attention to some kind of special dependence on *currents as signals*, often without a clear orientation to the broader field, referring instead to recent CM papers. Its use suggests a significant and valuable distinction over “conventional” solutions, perhaps in the hope that this perspective, with an element of novelty at the *cell level*, will influence circuit design in the stringent context of IC production. This paper asks: What factors unambiguously define a current-mode circuit, and formally differentiate it from standard realizations of some function? Can one point to any compelling, and in the most favorable cases unique, advantages? Are these cells clearly of general value, capable of widespread utility? These issues are examined from the critical viewpoint that *no circuits* carry the entire functional burden by the exclusive use of either currents or voltages, and very few fully exploit the specific, but narrow, benefits of CM concepts. Real-world product development invariably demands the vigilant and full embrace of what might be called the *Free Mode* perspective, but merely as a mnemonic, not a classification.

Key Words: current mode; analog design techniques

1. Introduction

This issue testifies to the continued interest in “current mode” circuits. The bibliography provided at its end, while far from exhaustive, shows that these concepts have a vigorous following. Yet, to the author’s knowledge, no *rigorous* definition of a current-mode circuit can be found in the literature. Since the term has been so widely employed, this should strike us as rather surprising. Its users presumably have something specific in mind, in choosing to identify their various contributions by appealing to this term, which was originally used to refer to a certain narrow class of techniques, without any attempt at a broader definition. Today, it all-too often appears to have joined the ranks of ambiguity, and become just another *good word*, along with *novel*, *universal*, *low power*, *high speed*, *low cost*, *high accuracy* and the like. When was the last time you saw a paper using the words *voltage mode* in its title? What special principle would it convey to you?

This ambiguity can be attributed to a casual, and often inappropriate, appeal to the term in publications, at times with insufficient regard for foundations de-

veloped decades ago, referencing instead recent and closely similar work. Its colloquial application implies the use of *currents as signals*, invariably with a tacit claim to a degree of *novelty*, announcing a *different*, and in some (unstated and unclear) way, *advantageous* implementation of a function formerly realized using other techniques. It hints at an ingenuous break with the traditional reliance on the use of voltages. But what is a *voltage-mode* circuit? Clearly, no circuit is deserving of this exclusive designation, since none operates in such a strictly-defined and limited manner. Some, like charge-coupled devices and switched-capacitor circuits, come close to operating in this “pure” mode, although in a practical taxonomy, it might be more appropriate to call these *charge mode* circuits.

Likewise, no circuit operates entirely in the current mode.¹ The literature shows that, in the majority of cases, the papers and letters concern the realization of some basic function at the *small-cell level*, the focus of the work, in which currents are reckoned to play a special role. The fact that the completed circuit (if ever considered) will, at some point in a *product* development, place equal reliance on signal voltages is

conveniently set aside. Indeed, essential voltages (later identified as state variables) frequently arise *within the cell*. This vision of “current mode” is far removed from the spirit of the first circuits that fell naturally into this class, which placed an essentially *exclusive* reliance on currents throughout a major portion of the signal chain, or as the variables realizing some special function. In such circuits, the supporting circuitry required to interface with the “voltage-mode world” was a trivial and unremarkable part of each complete, stand-alone solution.

1.1. The Relevance of “Analog Power”

Electrical theory concerns the conversion, transmission, transformation, control, storage, and utilization of *energy*. Electronic circuits address the origination, transmission, transformation, control, storage and utilization of *information-bearing* or *control signals*, in a kaleidoscopic variety of forms. All require the efficient utilization of power, although it is invariably minute in electronics; it usually plays no discernable role in circuit operation. Thus, in logic design, the emphasis is on voltage mode when considering logic signals at gate interfaces, and on current mode when considering their distribution. However, at the system level, a robust *information mode* prevails. The *incidental* power in thousands of logic gates will eventually raise challenges of thermal management, and in analog circuits self-heating can seriously threaten accuracy; but clearly, in no such cases is it a signal.

An obvious exception is transceiver design, where the power content of the signals is an *essential* aspect of the representation. An electromagnetic (volts-and-current) radio wave induces a minute amount of power on a receiving antenna, which is also responsive to the fundamental noise power kT of the surroundings. These define the power-signal-to-noise ratio (PSNR), whose preservation is crucial in processing these signals, involving amplification (by fixed- and variable-gain cells), frequency translation (by mixers), and the separation of the wanted carrier from others (by filters). Eventually, when extracting the signal’s payload, power considerations become secondary, and the voltage-mode viewpoint generally prevails during demodulation. In modern receivers, using digital modulation, information-mode takes over beyond this point.

In all cases where the preservation of PSNR is the primary consideration, the principles of impedance-

matching are identical to the load-matching rules essential to the efficient operation of a power-distribution grid. In impedance-matched systems, *both* the voltage magnitude and the current magnitude are of *precisely equal* importance. Thus, the nation’s distribution network and your cell-phone’s transceiver are compelling examples of the important *power mode* approach to design.

In a broader view, analog signals are electrical representations of temporal, dimensional quantities in the physical world. They are the continuous-time, continuous-amplitude and scaled *tokens* for a measured value (such as temperature, pressure, position); a control or actuating variable, an accurate reference source (voltage, frequency); a time base (in radar, TV, oscilloscopes, sonar); a stream of un-encoded audio or video; and much else. Throughout their processing chain, analog signals must have sufficient power to minimize errors, that is, considerably above the thermal noise power, kT . This evaluates to 4×10^{-21} W per Hertz of information bandwidth at $T = 290$ K, often stated as -174 dBm/Hz. Disregard for signal power, treating the signal as a pure voltage-mode or current-mode quantity, is a permissible convenience only when PSNR considerations can be neglected. This is less common than might be assumed, however. Regrettably, papers about current-mode circuits often omit any mention of their troublesome noise mechanisms.

1.2. The Dominance of Voltage Mode

For decades, the dominant signal representation mode has been in voltage form. This might sentimentally be identified with the advent of the triode vacuum tube. In grounded-cathode amplifiers, its grid voltage, with near-zero grid current, modulated the anode current. This was converted back to voltage mode by the anode load impedance for use by later stages: the tube current was an *incidental variable*. However, the persistence of voltage mode up to the present has much stronger practical justifications, chiefly in the matter of power sources. Voltages can readily be probed by instruments to be displayed and accurately measured without breaking circuit branches. Even when hiding behind a finite impedance, they can drive other compatible circuits with only a moderate effect on their magnitude; they are of obvious importance in both analog and digital practice.

Thus, for inverter-style CMOS logic in steady state, negligible current flows at its inputs or in the vertical branches of the cell. At moderate frequencies, its voltage-mode output can drive many similar gates without much concern about loading. While true, this view is, of course, just a convenient simplification. Transient current must flow at the input to alter the charge on the gate oxide and thus the channel current. The serious effects of load capacitance on the delay and transition times, particularly of the interconnects between gates, are well known. Such currents are clearly not signals; they are just an unavoidable aspect of circuit operation. Nevertheless, while incidental, logic design always requires rigorous consideration of how these current mode aspects are addressed.

1.3. *The Notion of State Variables*

The idea of incidental variables takes us closer to the heart of the matter. In CMOS logic, all the *state variables*, those necessarily appearing in the equations whose solution fully defines a circuit function, are voltages. Similarly, all state variables for a current-mode circuit must be currents; the incidental voltages caused by the presence of these currents are of minor interest. Thus: A voltage-mode (VM) circuit is one whose signal states are completely and unambiguously determined by its *node voltages*; a current-mode (CM) circuit is one whose signal states are completely and unambiguously defined by its *branch currents*.

Theoretically, it should make no difference which mode is used to realize a function; one is simply the dual of the other. Far less latitude prevails in developing practical products. Both circuit types are powered by voltage sources and perimeter interfaces are obliged to “speak voltage”. A current-mode realization might at first appear to be preferable, even when requiring significant alteration to the structure, and the (often inconvenient) use of current-mode interfaces.² But while a straightforward matter to recast signal processing operations in an alternate (VM/CM) style, there is no inherent guarantee, nor should there be any expectation, that either offers a clear and compelling advantage. The choice of the *local mode* is a pragmatic one, based on issues of convenience, the availability of known and trusted cell concepts, or the natural and comfortable fit of the cell within a product framework. Beyond the cell boundary, and often within it, the representation mode will generally change fluidly and frequently.

1.4. *The Practical Value of Duality*

The concept of duality relates to pairs of circuits having interchanged state- and incidental variables, while preserving the function. For example, in the LC tank of an RF oscillator there is a periodic exchange of energy between magnetic flux (current mode) and dielectric stress (voltage mode). There is a duality between a series-tuned tank, with its branch current as state variable, where the inner node voltage is incidental (although, as for all such variables, cannot be overlooked) and a parallel-tuned tank, having voltage as its state variable and incidental circulating currents. The supporting amplifier can optionally, and perhaps optimally, use a *local* current- or voltage-mode design viewpoint.

A primary voltage source is needed to support signal processing. With rare exceptions, current signals and biases in all types of circuit begin life as a voltages. This is not simply a matter of historical momentum. There is no practical dual for powering current-mode circuits. We do not start with a primary supply of say, 5 mA, and divide it up between the various parts of the circuit, accepting as incidental whatever voltages appear. Current-mode circuit schematics commonly show many ideal current sources, some of which are *dependent variables*, such as $(3x - 1)I_0$, where x is a normalized state variable. Often, there is little explanation (or none) as to how these are, or should be, implemented.

Such casual circuit notions cannot claim to be complete. Imperfections in these current sources, such as their finite conductance and capacitance, could mar the circuit’s utility. Performance details for any incomplete circuit should be interpreted with critical caution. One can find examples in the literature of current-mode cells whose *practical accuracy*, factoring in static, dynamic, matching and thermal aspects of these unspecified current sources, would probably be considerably poorer than reported.

Novelty has no intrinsic value. There is no merit in presenting an elegant-looking current-mode concept if the completed circuit requires the use of many auxiliary elements to meet practically meaningful objectives. When it is known that a proposed circuit is actually more complex than revealed, or that it under-performs what can be achieved by well-established means, one must doubt the legitimacy of its inclusion in the professional literature, except as a matter of curiosity. Circuits are not products; only the latter have the power to enrich our lives. Cells are merely the fragmentary servants of

a more complex set of down-to-earth practical needs, of value within the context of product design.

1.5. Sources—Voltage and Current

For decades, circuits have invariably relied on current sources to support their operation. Thus, in ECL, every logic gate needs a separate bias current, which is steered between transistors according to the logic state. ECL is an example of *current-mode logic* (CML). While this may be a convenient term for purposes of classification, the collector and base voltages play an *indispensable* role; they are not in any sense “incidental” (Fig. 1). Indeed, *all the state variables* in CML are voltages! The term *gm-mode logic* might be used, although the generic *current-steering logic* is more illuminating and precise.

References—fixed voltages or currents of known, accurate and stable value—are widely used in electronics. An impeccably accurate value is rarely needed, or provides any added value. Common exceptions are (1) in a system demanding *absolute* accuracy, having a voltage input and generating a *dimensionless* coded representation for display, storage, or use by another processor; and (2) where such a code is converted to a voltage of absolute accuracy. ADCs and DACs are familiar examples. But even here, absolute calibration is unimportant in many applications. In a well-integrated system it is often possible to use one voltage as a *common reference*, V_R , for an ADC (into DSP, say) and a subsequent DAC. Thus, the overall scaling does not significantly depend on V_R . Similarly, one can scale a function, say, a receiver’s RSSI voltage and a subsequent ADC from a common mediocre reference. Such *ratimetric* operation has many benefits [1].

References are needed whenever there is a translation to/from a voltage or current to an unrelated

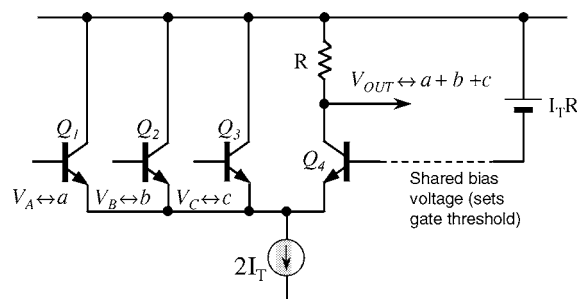


Fig. 1. A “current-mode logic” cell; all state variables are voltages!

dimension. Thus, a voltage-to-frequency converter (VFC) must conform to a function of the form³ $f = (V_{IN}/V_R)f_S$, where f_S might be defined by a CR time-constant. Here, V_R will often need to be very accurate. In a high-frequency VCO used in a PLL, absolute scaling is not needed, and V_R may be hidden in the built-in junction potential of a varactor diode. Likewise, the function of a linear current-mode multiplier/divider must have the general form $I_{OUT} = I_X I_Y / I_U$. In this case, I_U is required to be a reliable constant when used as a multiplier, and either I_X or I_Y when used as a divider.

Voltage is fundamentally the ratio energy/charge. The band-gap reference exploits the well-defined energy in a semiconductor, E_G , that is required to raise electrons from the valence band to the conduction band, expressed as a voltage by dividing it by the electron charge $q = 1.602 \times 10^{-19}$ C. In circuit design, it is defined as E_{GE} , its extrapolated intercept at $T_{ABS} = 0$. Within a given technology, this voltage has an almost invariant value, and thus provides a reliable basis for a voltage reference. In practice, access to E_{GE} is indirect: a band-gap reference circuit does not *inherently* provide this exact voltage. To provide a first-order temperature-stable output, typically about 1.23 V (slightly more than E_{GE}), the cell must be designed for a specific process [1].

The question arises: What equivalent *fundamental* mechanism can provide an accurate current reference? The distinctly different character of this quantity means that the accuracy of on-chip currents is inherently poor. They depend on semiconductor doping or film composition, on the cross-sectional area and length of devices, on temperature (ambient and that due to self-heating) and in some cases the applied voltage (resistance non-linearity) or bias on an associated junction layer (resistivity modulation). No physical effect allows the generation of a current to high accuracy, traceable to the Ampere, within a monolithic circuit. To realize a reliable current source, one starts with a voltage and arranges for it, or some fraction, to appear across a resistor. Monolithic resistors do not provide an accurate value as fabricated (a standard deviation of 10% is typical) and they have temperature coefficients that may be as high as $0.2\%/^{\circ}\text{C}$. Advanced analog-specific processes support thin-film resistors (SiCr or NiCr) of high stability (< 10 ppm/ $^{\circ}\text{C}$) which may be laser-trimmed to exact value.

In the dual view, current replication emulates the fan-out capability of the voltage-mode reference in

transposing currents from one part of a system to another. The preservation of accuracy here is not only a matter of careful matching and attention to device delineation, using integer or low-fractional ratios of unit devices, common-centroid layout techniques, and the like. Numerous mechanical and fabrication stresses must also be anticipated and in some way nulled. A variety of circuit modifications may be needed to raise the output resistance of these mirrors, and to ensure that these secondary reference currents are supply- and temperature-stable and insensitive to manufacturing tolerances.⁴

A single master current can optionally be generated by a high-accuracy off-chip resistor and replicated or changed in polarity using some type of current-mirroring system. For close matching of several currents, it may be better to distribute a voltage around the die and use emitter degenerated BJTs or large MOS devices in each cell. A better practice is to cluster the large devices into one bias block in the layout, and distribute their currents to the target cells, adding a small cascode transistor at the local level to radically reduce the capacitance and raise r_{OUT} ; a common base/gate bias line can be used for these.

While this kind of rigor is well understood by experienced designers of analog monolithic circuits, the “current mode” notions encountered in the literature all too often reveal little concern for these practical details, which are of crucial importance in nonlinear circuits design, where the bias values can affect the scaling of the function, cause signal-path distortion, or degrade conformance to a desired algebraic form.

1.6. Dynamic Range

The case for current-mode circuits is sometimes based on their presumed capacity to function over a larger range of signal values⁵ than in the voltage mode. The assertion is not without merit in special circumstances. Thus, a recent current-input logarithmic amplifier, based on the reliable translinearity of the BJT, accepts inputs from 10 pA to 10 mA, a nine-decade range (180 dB, but conservatively specified as 160 dB) and converts them to a decibel-scaled voltage with excellent absolute accuracy. However, a general argument for the preeminence of current-mode processing is not so easily made [2].

The smallest discernible signal is limited either by offsets or by noise. In the most favorable scenarios, the

peak signal amplitude in voltage-mode circuits is limited by the supply voltage, which may be dictated by the maximum permissible terminal voltages on the active elements. As process technologies continue to emphasize packing density and speed, the analog qualities of transistors are degraded and the reduction in voltage swings is severe. It is common to use supply voltages of 2.7–5.5 V, although many consumer products allow only 1.5 V or even less for their supply. Differential signal representations are valuable in easing this constraint. For the present comparative purposes, we can take the upper end of the voltage swing as lying roughly between 0.5 and 5 V *pk-pk*.

The lower end of the dynamic range is harder to quantify. In *DC systems*, offset voltages may set the limit. Using trimming, this may be as low as a few microvolts; in commodity-grade products, one may have to settle for worst-case values as high as 5 mV. Thus, the dynamic range of a DC-coupled circuit in an optimistic scenario might be, say, 5 V/5 μ V or 120 dB, while in a pessimistic scenario it might be as low as 0.5 V/5 mV or 40 dB—a 10,000:1 range of possibilities! In DC-coupled systems, wide-band noise can be removed by aggressive filtering, but $1/f$ noise will often limit this range.

The *AC dynamic range* of a voltage-mode circuit is determined by its internal noise voltages, many of which are generated by *noise currents* associated with the active elements. The wide-band noise-spectral-density (NSD) depends on many biasing details and device parameters. The total noise depends not only on the information bandwidth (that is, the Δf), but also on the absolute frequency range (that is, whether $\Delta f = f_1 - f_2$ or $f_3 - f_4$). It increases at low frequencies, as flicker noise intrudes, and again at high frequencies, where device power gain falls and secondary sources assert an influence.

For example, consider a BJT differential pair used as the transconductance in the first stage of an open-loop amplifier, biased with a fixed tail current $2I_T$ of 1 mA (Fig. 2a). Assuming a total input-referred resistance of 100 Ω , the voltage-noise-spectral-density⁶ at this current is ~ 1.6 nV/ $\sqrt{\text{Hz}}$. For a peak input swing of ± 15 mV (~ 10 mV RMS; higher input levels would generate excessive distortion in this simple cell) and an information bandwidth of 1 kHz, the dynamic range would be $20 \log_{10}\{10 \text{ mV}/(1.6 \text{ nV} \times \sqrt{1000})\}$, or 106 dB. However, when this same cell is used as the transconductance input stage of a unity-gain closed-loop amplifier, where the input/output signal swing

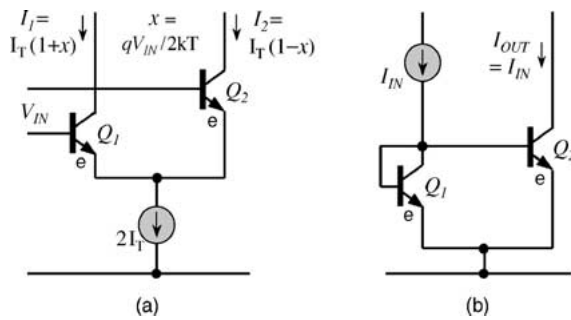


Fig. 2. Basic analog building blocks.

could be more than ± 4 V (~ 2.8 V RMS) using dual 5 V supplies, the dynamic range is immediately extended by $20 \log_{10}(2.8 \text{ V}/10 \text{ mV})$ or 49 dB, to 155 dB; and if the at-frequency open-loop gain of this amplifier is high, the tanh-induced distortion becomes negligible. The dynamic range of voltage-mode circuits can be extended even further, depending on the signal frequency and permissible distortion limit, to over 180 dB in many transducer applications.

What is the equivalent dynamic range for a current-mode circuit? Such comparisons can never be definitive. For example, DC offsets may impose a limit on the dynamic range of a DC-coupled amplifier, while their effect in a translinear multiplier or VGA cell might be to cause even-order distortion.⁷ A basic BJT limitation is that due to shot noise. For a collector current of I_C this is $\sqrt{2qI_C}$ per $\sqrt{\text{Hz}}$. The current-mode noise-limited dynamic range, assuming negligible resistances, is therefore $I_C/\sqrt{2qI_C}$, or $\sqrt{I_C/2q}$, which evaluates to 135 dB/ $\sqrt{\text{Hz}}$ at $I_C = 10 \mu\text{A}$. For the 1 kHz bandwidth as used in the previous example, this amounts to 105 dB.

However, few if any practically-useful current-mode functions can be achieved with a single transistor. In all studies of dynamic range, a quality so freely interpreted and offered as evidence of a cell's value, one must specify exactly how the term is being used, the specific circuit function, its detailed configuration, many of the relevant device parameters, and all operating conditions. In this regard, "current-mode" notions are often presented with insufficient clarity or precision to assess their practical value.

Consider the noise-limited dynamic range of a basic unity-gain current mirror, Fig. 2(b), comparable in utility as a current-mode building block to the differential pair in voltage-mode. Using ideal BJTs, having

high beta and no junction resistances, each transistor exhibits an uncorrelated peak SNR (each bias current divided by each noise current) of $\sqrt{I_{IN}/2q}$. The overall SNR is thus simply $\sqrt{I_{IN}/q}$. In practice, the junction resistances associated with the base ($r_{bb'}$) and emitter ($r_{ee'}$) influence the overall current noise. It is readily shown that, for this mirror, the dynamic range benefits from emitter resistance (whether internal to the transistor or added as emitter degeneration) increasing at an asymptotic rate of 10 dB/decade above the corner $r_{ee'} 2 > kT/qI_{IN}$. On the other hand, the dynamic range *decreases* at the same asymptotic rate above the corner $r_{bb'} > kT/2qI_{IN}$.

It would be easy to continue such armchair explorations to discover various optima and desiderata. However, it is inadvisable to explore only those academic aspects of behavior that just happen to be conveniently tractable, to the neglect of the broader view, involving less-readily quantified effects in the fully-modeled device, or demanding the solution of frustrating nonlinear equations. It is likewise unproductive to dwell on *local* optimization, with insufficient concern for performance limitations elsewhere in the signal path.

2. Mode Transformations

All analog design has a consistent theme: the liberal use of translations from one signal representation to another, reflecting the innate necessity of what is here called the *free mode* perspective. Signals undergo natural and fluid mode transformations through the portals of conductance and resistance, at low frequencies, or of admittance and impedance, whenever the signal frequencies are high enough for device inertia to exert a significant effect. These bridges from one mode to another are provided by the active elements, often supported by passive components, for a variety of excellent reasons. Wherever at least one time-constant is involved (whether deliberate or incidental) mode transformations are inevitable. On these fundamental grounds, we cannot speak of a "current-mode filter", a "current-mode integrator", a "current-mode oscillator" and the like.

Conversion from voltage to current mode requires an admittance or a transadmittance element (more familiar in the guise of transconductance, at low frequencies). Similarly, transformation from current to voltage mode requires an impedance or a transimpedance

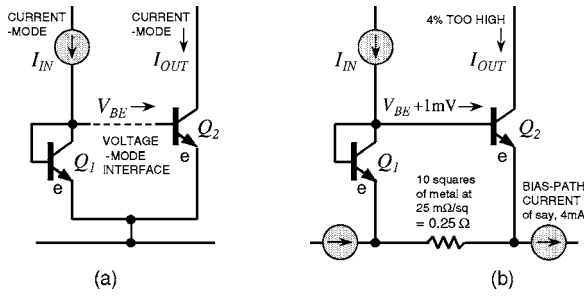


Fig. 3. Some voltage-mode aspects of a current mirror.

(transresistance, at low frequencies). In practice, much of the design effort will be put into minimizing the distortion caused by the inherent $V-I$ nonlinearities of the active elements, and in coping with transistor mismatches and their temperature sensitivities. Thus, both bridges generally include resistors.

In the current mirror (Fig. 3(a)) the nonlinear, frequency- and temperature-dependent (NLFTD) impedance of Q_1 converts the current I_{IN} to a NLFTD voltage, $V_{BE}(I_{IN}, f, T)$. This is applied to like device Q_2 which responds as a NLFTD transadmittance to generate I_{OUT} . Using currents at both input and output, this is regarded as a “current-mode” cell. But the voltage at the input node may be ignored only if I_{IN} is provided by a perfect current. The NLFTD of the mirror precludes this flippancy when the source of I_{IN} has finite admittance. Furthermore, for Q_2 the precise value of this voltage is crucial: it must be within $\sim 250 \mu V$, a tolerance of roughly 0.03%, for a 1% error in I_{OUT} .

In the schematic, emitters (and sources) should be shown as connected locally and grounded through a single branch, to remind the layout designer to avoid metal routing mistakes that could introduce spurious voltages (Fig. 3(b)). These can have painful consequences, underscoring the voltage-mode *alter ego* of the mirror. Non-degenerated BJT mirrors should be used sparingly, and only where low accuracy and high noise are permissible. However, the benefits of degeneration cannot be used when I_{IN} has a wide range of values or when the output must swing to almost the supply rail. Figure 4(a) shows a mirror⁸ that addresses both desiderata. It is an example of a class called *Voltage-Following Current Mirrors* [3, 4]. The *V-mirror* exemplifies the free mode aspects of practical cell design. (Notably, this term combines *voltage* and *current* in the one expression). A low voltage gain in its rudimentary op amp is sufficient, since the change in V_{BE} is already small, being 60 mV/decade of I_{IN} ; more important is a low offset voltage. Its bias currents do not affect I_{OUT} , since i_{B2} is canceled by i_{B1} . By a simple design modification in the op amp, i_{B2} is arranged to be κi_{B1} when $Q_2 = \kappa Q_1$.

The *V-mirror* has interesting properties. If I_{IN} were truly a current source, its r_{OUT} would in be principle infinite⁹ even for low Early voltages in Q_1/Q_2 , since their collectors are equally biased to V_{OUT} . This makes it attractive for loading a preceding cell, having a pair of output currents whose balance depends on *its* collectors being equally voltage-biased. With a load resistance R_L added, $r_{IN} = -R_L$; thus, an increase in I_{IN} causes the voltage at node *a* to decrease. In a simple

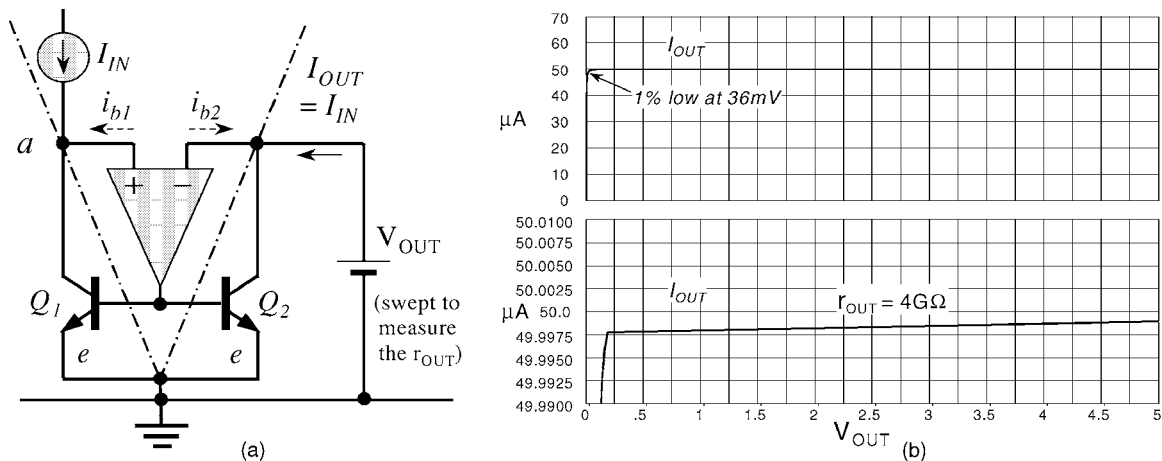


Fig. 4. The *V-mirror*: A BJT super-mirror reflecting the free mode perspective.

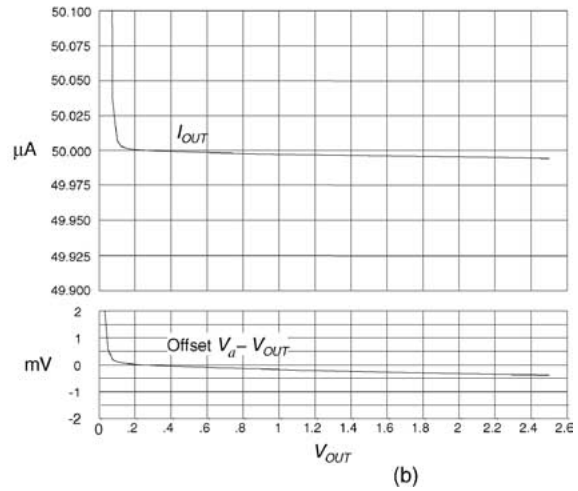
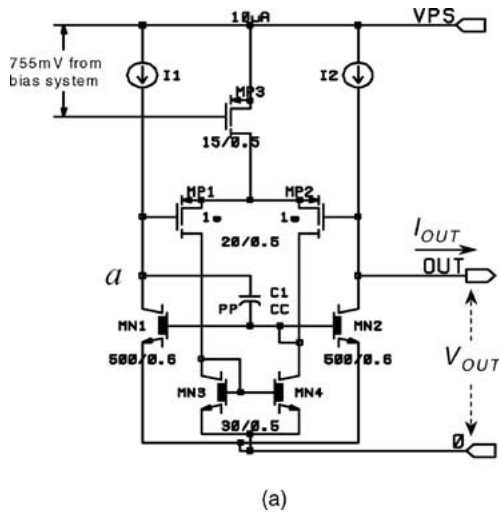


Fig. 5. A CMOS version of the V-mirror.

mirror, as the V_{CE} of Q_2 drops below ~ 150 mV its base current rises rapidly, robbing I_{IN} which causes I_{OUT} to fall precipitously. Here, with the base currents provided by the amplifier, I_{OUT} remains accurate down to very low values of V_{OUT} , even though the transistors are in deep saturation (Fig. 4(b)). Equal emitters are used in this illustrative simulation, and the op amp's voltage gain is ~ 300 . Other Q_1/Q_2 ratios can be used, over a wide range, with the same cancellation of V_{AF} errors.

Most examples in this paper use BJTs, but MOS/BiCMOS versions are usually possible with little change. Figure 5(a) shows a CMOS version of a V-mirror on a $0.35 \mu\text{m}$ process, connected as a differential-to-single-sided converter: $I_{OUT} = I_2 - I_1$. The output error is 1% at $V_{OUT} \approx 55$ mV (Fig. 5(b)). The 3 dB bandwidth for $I_1 = 100 \mu\text{A}$, $I_2 = 150 \mu\text{A}$, $V_{OUT} = 1$ V and $C_C = 1.5$ pF is 180 MHz. In these baseline simulations, device matching is assumed to be perfect. The use of large transistors and common-centroid layout practices is advised.

2.1. Mode Transformations in an Op Amp

While an op amp is correctly classified as a voltage-in, voltage-out element (formally, a voltage-controlled voltage-source, VCVS), it should not, contrary to the prevailing popular view, be regarded as a "high-gain amplifier with limited bandwidth". Rather, its open-loop transfer function is essentially that of an integrator: $V_{OUT} = V_{IN}/sT$, where T is its character-

istic time constant. The open-loop gain at a signal frequency f is defined by T , having a magnitude of unity at $f_1 = 1/2\pi T$, and f_1/f at lower frequencies, over a range of many decades below f_1 . Thus, a loosely-named "10 MHz" op amp will have a voltage gain V_{OUT}/V_{IN} of only 10 at 1 MHz. The asymptotic open-loop DC gain is rarely of importance, even when used at high closed-loop gains.

Whenever we encounter a time constant in a circuit function, we need to consider very carefully what defines it. In a typical monolithic op amp (Fig. 6) it is defined by the product of a (real) on-chip resistor and on-chip capacitor. The resistor is implicated in determining the bias current I_O , and thus the transconductance (g_m) of its input-stage transistors; then the capacitor C_C defines the unity-gain angular frequency $\omega_1 = g_m/C_C$. The gain-bandwidth product

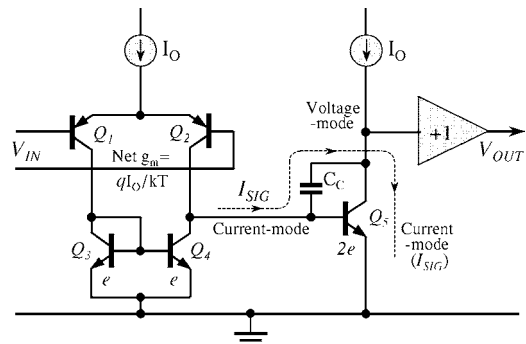


Fig. 6. Mode transformations in an op-amp.

of practically all monolithic op amps is very poorly defined; consequently, so is the open-loop gain at frequencies above a few Hertz. This key fact is curiously underemphasized in treatments of op amp application.

Let's follow the mode transformations for this implementation. While rudimentary, the essentials remain the same after elaboration. Indeed, this actual circuit is of widespread value as shown; using care in device sizing and balance, the inputs may operate down to ground. The differential voltage-mode signal V_{IN} is transformed to a pair of current-mode signals by the I_O -determined transconductance, g_m , of the input stage. These two currents are then "weighed in the balance" of a current mirror, and remain in current mode at its terminals (although as noted, two mode transformations occur internally in any mirror).

The difference I_{SIG} is applied to the voltage-gain stage, a grounded-emitter transistor, Q5, biased at a constant I_C . The difference current I_{SIG} from the mirror flows almost entirely in C_C (neglecting here the C_{JC} of Q5). At this point, an important mode transformation occurs. It has the form of current-to-voltage, but not due to a transresistance. Rather, it is due to the frequency-dependent impedance of C_C , that is, $j/(2\pi f C_C)$. The signal, now back in voltage form, is buffered by a unity-gain output stage, usually capable of delivering a moderately large load current, I_L . The amplitude of this output voltage is $g_m/2\pi f C_C$ larger than the input, with a constant phase lag of 90° over a wide range of frequencies. Thus, two major and two minor mode transformations of the signal have occurred in this extremely simple signal path, having the free-mode state variables V_{IN} , I_{SIG} and V_{OUT} .

2.2. Definitions and Criteria

A Working Definition is as follows: *A current-mode circuit is one in which the state variables are exclusively in the form of currents.* This allows for the fact that, in all real examples, there will, and must be, *incidental* voltages in the circuit. However, these do not appear in the describing equations of the top-level function; they are invariably scaled arbitrarily, and often exhibit high temperature sensitivities. The V_{BE} in the current mirror is such an incidental variable. While a mirror may be conveniently regarded as a current-mode cell, it will be clear that from the circuit's viewpoint, this particular voltage is *crucially significant*, being the precursor of the current-mode state variable to follow.

An abbreviated dual of these statements would be: *In a voltage-mode circuit the state variables are exclusively in voltage form.* In every practical case, there will be incidental currents. These are invariably scaled arbitrarily while not affecting the overall scaling of the function. The load current, I_L , in a practical realization of the output buffer of Fig. 6 can be regarded as an incidental variable from a cursory perspective. However, like the V_{BE} of the mirror example, this current could be very significant, in determining the buffer's voltage gain, consequently the magnitude of the voltage-mode state variable which is the output, and the amplifier's open-loop gain at all frequencies down to zero.

2.3. Key Criteria

Legitimate examples of current-mode circuits can be identified by asking these questions:

- (1) Does the Working Definition apply? that is, are all of the state variables in current form? or more generously, the *majority* of them?
- (2) Is the essential function independent of any deliberately-introduced time constants?

It is reasonable and informative, though not necessary, to add these auxiliary questions:

- (3) Is the circuit, and its presentation, *complete* in sufficient detail, that is, not dependent on any unspecified supporting agents, such as the particular values of bias currents, or special functional derivatives of the state variables, such as $(3x - 1)I_O$?
- (4) If the circuit is addressing some function formerly implemented using voltage mode practice, does it offer any *compelling and defensible advantages* over the prior art, or does it merely replicate such a function in a different, and perhaps interesting, way?
- (5) Have the circuit's special merits been recognized and realized by *other designers*? Has it become *widely adopted in actual products*, on the basis of these unique merits? If of a totally new form, is such an outcome likely, with the fourth criterion in mind?

These criteria may appear to be overly strict. Certainly, much that has appeared in the literature as "current mode" would not qualify. The first to be challenged

would probably be the last one, testing the *practical utility* of a “novel approach”. But for the designer of products—which must be complete, robust, high-yielding in mass production, inexpensive, benign, free of artifacts, insensitive to supplies and temperature—this is the *only important criterion*. A current-mode circuit, just like any other, must *earn* its reputation through widespread use, or risk being soon forgotten, along with hundreds of other curiosities that fill the pages of our proceedings, transactions, letters, and journals.

3. Examples of Current-Mode Circuits

In the mid-1960’s, the author discovered a class of circuits, retrospectively satisfying the first four of the above criteria, and for which he coined the term “Current Mode”. Within a decade, the last criterion was met in full.¹⁰ The first of this new family of cells arrived in the following way. BJT current mirrors and differential pairs were in wide use in 1965. As a linear-circuit element, the mirror was a truly new form. Its topology was not found in vacuum-tube design. Tubes require a negative grid bias to reduce the anode current to near-zero, which would not naturally arise if they were used in place of BJTs.¹¹

By contrast, the differential pair is a *mode-transforming element*. An input voltage, V_{IN} , applied between the bases unbalances the collector currents, making an output I_{OUT} . Unlike the mirror, this *could* be realized in vacuum-tube form, and was, in op amps widely used in control systems and analog computers. It was called a *long-tailed pair* (LTP) because the bias current for the cathodes was provided by a high-value resistor (the “tail”) taken to a large negative voltage. The BJT-LTP had a serious flaw: its I_{OUT} vs. V_{IN} relationship is very nonlinear, having the form $\tanh(qV_{IN}/2kT)$, with a quasi-linear region of a few millivolts. But its transconductance is an almost exactly linear function of the tail current, a property later identified by the name *translinear*. This was useful at a time when analog multiplication was still of broad general value. Its potential was of specific interest to the author in 1966, for use as the core of a 500 MHz variable-gain amplifier [5]. BJT-LTP cells remain at the heart of many contemporary VGAs, sometimes using another circa-mid-1960’s linear transconductance concept, the multi-tanh principle [6].

The question arose: Was there some way of merging these two basic cells to realize a super-cell, having

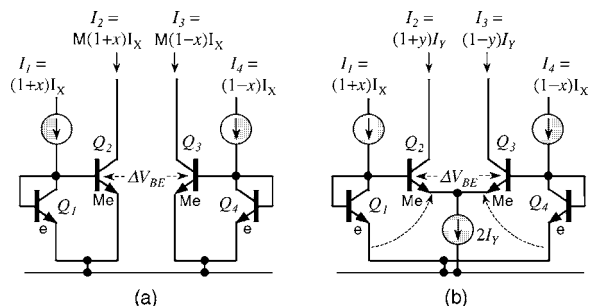


Fig. 7. From current mirrors to current-mode multiplier.

the *linearity* of the fixed-gain current mirror but the *variable-gain* properties of the differential pair, exploiting the excellent linearity of its transconductance value with respect to the gain-controlling (tail) current? It became apparent that this was not only possible, but effortless and natural, leading immediately to a *current-mode analog multiplication element that was linear with respect to both of its inputs* [7]. This one-step metamorphosis is shown in Fig. 7. In (a) we have two independent mirrors, side-by-side; the choice of *complementary* input currents will later become apparent. The outputs are simply linear replications of the inputs, with or without a current-mode gain/loss factor, depending on the ratio M of the emitter areas¹² $Q2/Q1$ and $Q3/Q4$.

Now cut the path from the inner emitters to the ground node, join them, and provide them with a bias current $2I_Y$, as in Fig. 7(b). With this one, tiny change in topology, we have transformed the inner transistors from being the “hind legs” of two separate mirrors, into a differential pair, resulting in a genuinely new current-mode element with surprisingly broad and valuable properties. Both of the cell’s signal inputs—the state variables $2I_Y$ and the dimensionless *modulation factor* x —and its signal outputs $\pm yI_Y$ are in current mode.

The voltage, ΔV_{BE} , generated between the inner bases is *incidental*. If the world were kind enough to supply all signals in current form, the variation of this voltage with signal currents and temperature would have essentially no bearing on the operation and utilization of this cell. In practice, as when the currents I_1 and I_2 are generated directly by voltage inputs via resistors, the ΔV_{BE} will frequently intrude into the overall circuit behavior. It is of enough importance to give it a special name: the *characteristic voltage*. This term was coined to refer to any situation in which two transistors have a common emitter (source) connection

and operate at unequal collector (channel) current-densities. For the BJT, it is:

$$\Delta V_{BE} = \frac{kT}{q} \log \frac{I_1}{I_4} = \frac{kT}{q} \log \frac{I_2/M}{I_3/M} \quad (1)$$

The mirror ratio M cancels out, and no longer determines the gain. In practice, it would be made closely equal to I_Y/I_X , using a mean value of I_Y when this is a variable. The key property of this cell is that the *ratio* of the currents in Q2/Q3 replicates that in Q1/Q4. This follows directly from Eq. (1), assuming all transistors are operating at a common temperature.¹³ This relationship may be stated in quotient or product form:

$$I_1/I_4 = I_2/I_3 \quad \text{or} \quad I_1 I_3 = I_2 I_4 \quad (2)$$

Using the complementary currents shown,

$$(1+x)I_X(1-y)I_Y = (1+y)I_Y(1-x)I_X \quad (3a)$$

which collapses to

$$y = x \quad (3b)$$

The differential input current is $I_{IN} = (2x-1)I_X$ and the output is $I_{OUT} = (2x-1)I_Y$. Thus, we can state the function in product form

$$I_{OUT} = (I_{IN}I_Y)/I_X \quad (4a)$$

or in “variable gain” form

$$I_{OUT} = G_{CM}I_{IN} \quad \text{where} \quad G_{CM} = I_Y/I_X \quad (4b)$$

3.1. The Evolution of Translinear Cells

This was the first example of a large class of nonlinear current-mode circuits. The extension of this basic topology to four-quadrant multiplier operation was straightforward [5] and has been widely used. Scores of other such cells quickly followed [5–7], numerous patents, and doctoral theses, notably that of Seevinck [8], which cataloged all the then-known cells as well as examples of formal synthesis methods. In 1975, the author proposed a formal definition of this class of circuits, based on the *strict translinear* (STL) principle [9], in which all state variables are currents, and all voltages are incidental.

In recent years, many papers [10–12] have exploited similar principles using MOS in weak inversion, where $I_{DS}(V_{GS})$ takes on an essentially exponential form. In sub-micron CMOS this regime extends to useful current levels (microamps). The large V_{GS} offsets in small devices limit the accuracy of such cells; the use of much larger transistors to avoid this problem penalizes circuit speed. In the main, these papers report on the performance of MOS in previously-known BJT topologies. Further branches of the evolutionary tree include the idea of dynamic translinear cells [13] and log-domain filters [14, 15], although here the inclusion of time-constants precludes classification as “current mode”. However, these extensions do not use STL, but exploit the concept of *general translinearity* [16].

In another evolutionary direction, MOS transistors are used in strong inversion [17]. The common assumption of quadratic behavior in this regime is incorrect, casting serious doubt on any analysis based on this approximation. A further concern seen in analyses of CMOS “current-mode” circuits is the simplifying assumption of the $I_{DS}(V_{GS})$ behaviour for a constant drain voltage, whereas the device behavior is often significantly altered by the voltage swings at this terminal, due to the varying V_{GS} of subsequent (driven) cells. Modern devices exhibit a strongly varying functional form of $I_{DS}(V_{GS})$ over a range of I_{DS} , even when $V_{DS} \gg V_{GS}$. Thus, in an analysis of sufficient rigor for practical purposes, many device parameters persist in the equations defining the circuit function, that is, these voltages become relevant state variables, strongly coloring the function of the cell.

The most stunning aspect of Eq. (2) is the number of BJT and circuit parameters that instantly disappeared, being independent of bias levels, temperature and emitter area.¹⁴ Even the semiconductor material is unimportant: the equations are equally valid for pure Ge or Si, and for SiGe, GaAs or other HBTs. The ascent of BiCMOS as the process of choice for future mixed-signal ICs will preserve these benefits of BJT current-mode cells.

3.2. The Importance of Interfaces

The valuable properties of basic CM cells have been widely exploited in products during the past three decades. However, this broad appeal should not be attributed to the fact that they locally operate in the current mode. While interesting, this is but another

incidental factor; isolated cells serve no-one's practical needs. They are only a starting point, the rudimentary *cores* of complete, application-ready products. Furthermore, even within translinear CM cores, their *intrinsic voltage-mode aspects* require close attention to achieve high accuracy and low noise. In many contemporary cases where these cells are used, still in their original forms, it is apparent that this rigor is not always observed.

The diversity of these products arises in the way in which the near-universal requirement for them to slip effortlessly into a *voltage-mode world* have been addressed. This is the function of the *supporting circuitry*, where the greatest novelty is required, and in which individual solutions branch most widely. And, with few exceptions, it is where all the genuine performances advances are to be found, as demonstrated in Section 3.6. In some cases, such as high-speed/high-frequency/low-noise products, designers are obliged to also pay attention to *power-mode* and *impedance-mode* aspects. But in every case, they are pursuing the practical and unavoidable necessity of the *free-mode* perspective.

3.3. Two Seminal Cells

The fundamental relationship stated in Eq. (2) can also be obtained from a second four-transistor core. Figure 8 shows the fixed, essential connections that define these two seminal forms. It is only changes in the supporting circuitry that determine the functional variety of all such elaborations. These include the methods by which the input currents are accurately forced in the *collectors* of Q1 and Q2 (using other than the customary diode connections); the way the outputs I_1 and I_2 are utilized; the development of the ΔV_{BE} in (a), and the generation of bias currents to provide an accurate CM gain, having

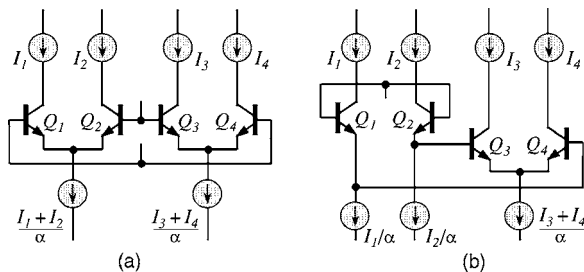


Fig. 8. The primitives of two general-purpose current-mode cores.

either a linear or a linear-in-dB (exponential or reverse exponential) relationship to a control voltage; and so on. Note that I_1 and I_2 can also be outputs, in either form. The inclusion of the transistor alpha in the lower currents in these figures is only a reminder that they are not precisely equal to the sum of the upper currents.

It cannot too strongly be emphasized that, in competitive product design, it is this *mode-transforming* supporting circuitry that calls for the greatest ingenuity. This includes the choice (often, invention) of compact and efficient topologies, where the function of every element can be fully justified; optimal device scaling and biasing; the weighing of trade offs; attention to numerous issues of robustness, manufacturing, testability, packaging; and so on. Depending on such particulars, the Fig. 8 cores might be expanded into fixed-gain current-mode amplifiers; fixed-gain, active-feedback voltage-mode amplifiers; many varieties of variable-gain amplifier; multipliers and dividers; squaring and square-rooting circuits; RMS-DC converters; and much else.¹⁵ We can classify these as *developed current-mode cells*. When this work is completed, and all the perimeter connections to a current-mode cell have been finally tied to their proper places, the working schematic will put even the most sophisticated of current-mode cores into proper perspective.

3.4. An Illustrative Current-Mode Amplifier

Figure 9 shows an essentially complete CM amplifier. Only the biasing cells, providing two voltage rails for the degenerated PTAT and ZTAT current sources, are omitted for clarity. The thin-film resistors of the 25 GHz CB-SOI process ensure high temperature stability of performance parameters. All internal state variables are in current form. The simple interfaces provide direct interfacing with voltage signals; the first stage behaves as a linear transconductance for V_{IN} while the output currents are converted to V_{OUT} by the 25 Ω load resistors R_{L1} and R_{L2} (so the differential output resistance is a fairly pure 50 Ω). The peak (clipping-level) output is 3.2 V pk-pk, using a single 2.7 V supply. Optionally, with $R_{L1} = R_{L2} = 50 \Omega$ and $R_L = 100 \Omega$ the available linear power is >10 mW.

The core is little more than three NPN current mirrors, having current gains of 6, 34/6, and 190/35, a total CM gain of $\times 185$, supported by PNP sources whose degeneration minimizes noise and offsets in the signal-path. While the actual current values do not

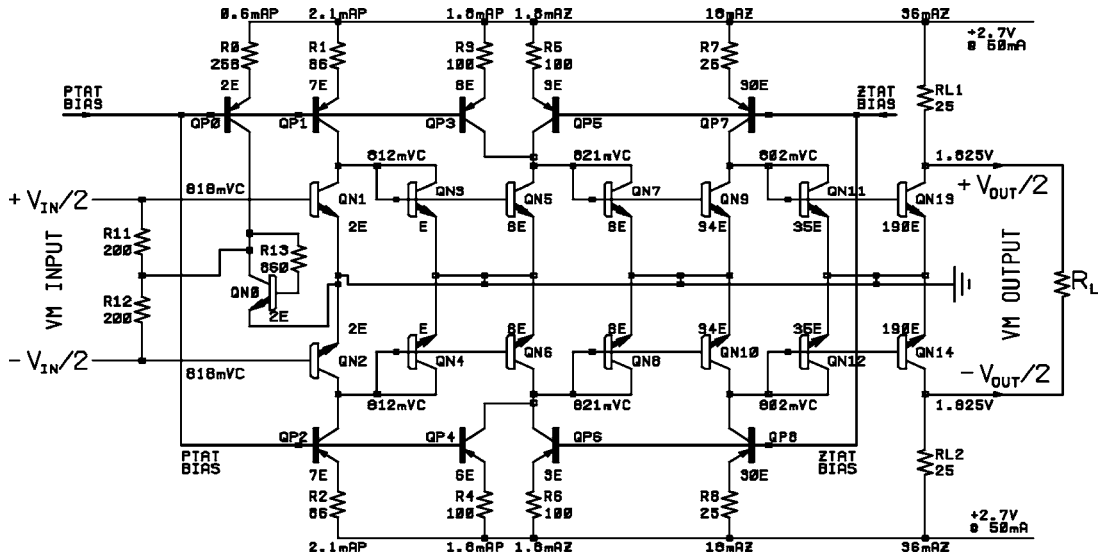


Fig. 9. A fully-designed current-mode amplifier.

significantly affect the CM gain, the use of both PTAT and ZTAT (zero-TC) currents ensure a temperature-stable overall *voltage-mode* gain of 48 dB (that is, $\times 251$, increasing by only 0.18 dB over a supply range of 2.7–3.3 V), and a constant peak output capacity. With reduced emitter degeneration, operation down to 1.2 V is readily achieved.

The simulation results of Fig. 10 show the DC output and incremental gain at 10 MHz, vs. V_{IN} over ± 6 mV. The deviation from an end-point fit (static nonlinear-

ity) is 0.025%, essentially independent of temperature. The AC gain at -40° and 90°C increases by $+0.01$ dB from its 25°C value; the small change ($+0.075$ dB) at the extremities of the V_{IN} range demonstrates good AC linearity.¹⁶ Figure 11 shows the AC response and the input-referred voltage noise spectral density (VNSD). The -3 dB bandwidth is constant at 255 MHz; the gain-bandwidth product is thus 64 GHz. The phase response is essentially linear up to 200 MHz. The unloaded output noise at 25°C for an information bandwidth of

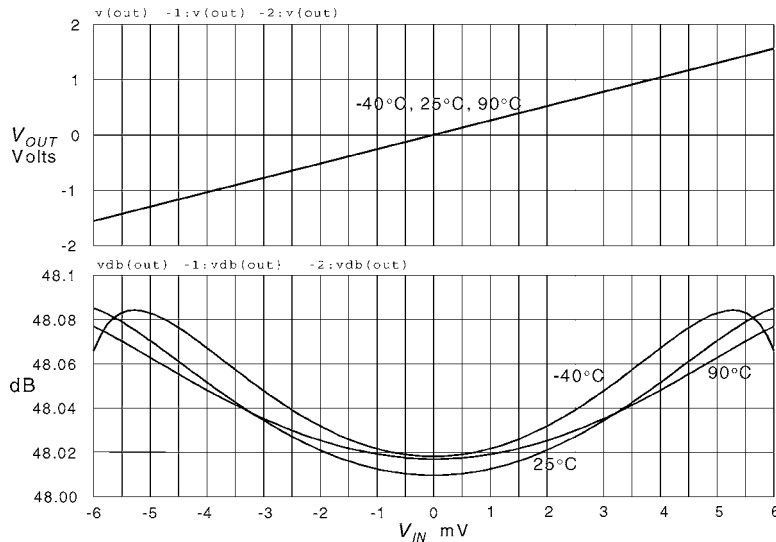


Fig. 10. DC output and AC linearity of current-mode amplifier.

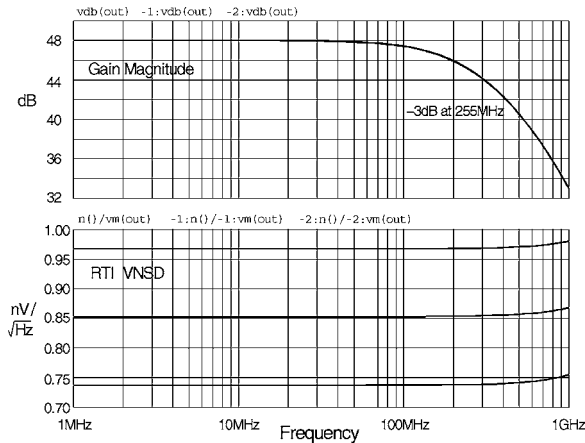


Fig. 11. Gain magnitude and input-referred VNSD for current-mode amplifier.

1 MHz is $\sim 200 \mu\text{V}$ rms; for a signal output of 1 V rms, the dynamic range is ~ 74 dB.

3.5. Recent Extensions of CM Cells

In a flurry of excitement during the late 60's, numerous BJT-CM cells were developed. Since then, very few distinctly novel *strict-translinear* cells have appeared. The advent of well-balanced complementary bipolar (CB) processes has added some variety to CM cell topologies, for example [18, 19, 21], but the advantageous adoption of these core cells into commercial products, as reported in the public domain, appears to be minimal. Taking full advantage of CB on silicon-on-insulator (SOI) technologies, which provide true three-terminal transistors, the sophistication of the supporting circuitry that can clothe simple cores with standard voltage-mode interfaces has continued to show ingenuity, again underscoring the observation that "circuits (cells) are not products".

The progress in log-domain (translinear) filters has also been aided by the advent of CB. In one realization of the form [20], the key cell shown Fig. 12(a), a voltage-controlled current-mirror, is used for tuning the filter at each basic integrator stage. This cell is of pre-CB vintage [2], using substrate PNPs. But in failing to meet the first two criteria, log-domain filters are clearly not examples of CM design. In fact, all filters must necessarily operate in a free mode fashion, since there is an essential interplay between voltage-mode and current-mode state variables. Figure 12(b) shows another useful mirror [6]. As in the last example, it pro-

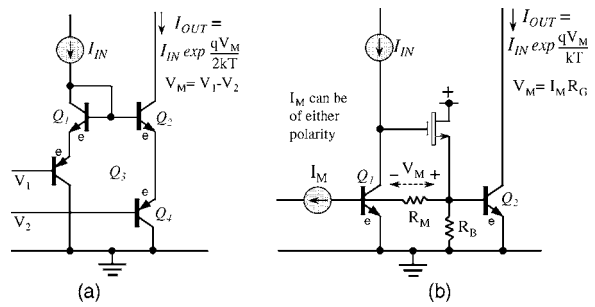


Fig. 12. Voltage- and current-controlled current-mirrors.

vides an independent port for a *linear-in-dB* variation of the mirror gain (V_M is scaled 3 mV/dB at 300 K), but this time using a *current* as the control variable. While these two mirrors are based on the same principles, the use of currents at all of the boundary terminals in the second example clearly puts this particular realization into the class of current-mode circuits, meeting all five of the proposed criteria.

3.6. A Highly-Developed Translinear VGA

To further demonstrate that performance advances and circuit novelty in products using a current-mode core are invariably found in the supporting *free-mode circuitry*, Fig. 13 outlines the structure of a voltage-in/voltage-out variable-gain amplifier. Its core is essentially the familiar cell of Fig. 8(a), but with some important modifications, not shown here. Its CM signal gain is simply I_N/I_D , and is closely specified over a range of > 100 dB. The denominator current, I_D , and the numerator current, I_N , are independently controlled by voltages V_G and V_M , respectively, applied to high-impedance interfaces.

This VGA is designed to manage a wide range of input voltages (from the noise floor to ± 4 V). A *linear-in-dB* gain law is desirable, and is essential as a practical matter with a large gain span. I_D has an accurately-scaled exponential response to V_G , the primary gain-control voltage of 0 to 1.5 V, scaled 30 mV/dB. A logic input allows the gain to either increase (0–50 dB) or decrease (50–0 dB) with V_G ; both modes are needed in contemporary applications. On the other hand, I_N , thus the overall gain, increases linearly with respect to V_M . This also allows the peak output voltage to be accurately set, useful in driving an ADC. V_M defaults to 0.5 V, for a peak output of ± 2 V; at its maximum value of 5 V, the gain is 20 dB higher and the

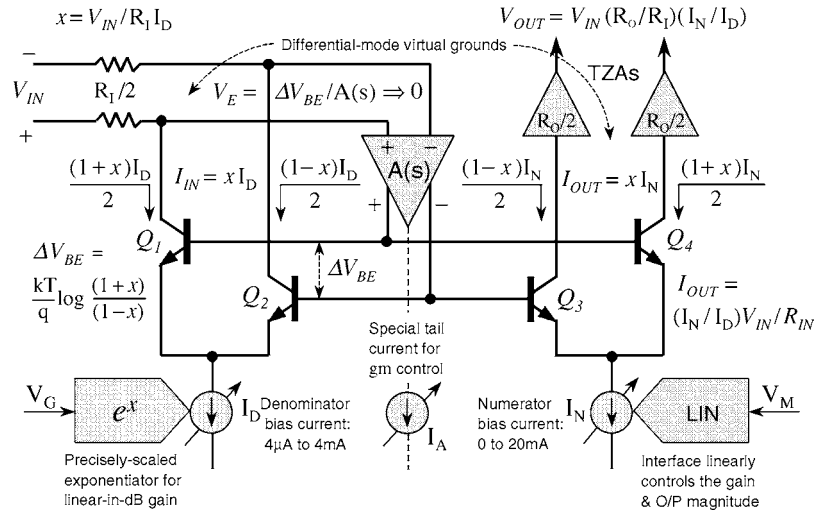


Fig. 13. Basic structure of a high-performance variable-gain amplifier.

differential output is then limited by the supply, V_S , (2.7–6 V) and the rail-to-rail drivers, to $\pm(V_S - 0.5 V)$. The input-voltage capacity, output amplitude, overall gain, AC response, and scaling of all control interfaces are temperature-stable.

Based on the diverse performance objectives for this product, the 25 GHz CB-SOI process was used. The internal structure of this enhanced core and its voltage-mode aspects were key to addressing these issues. Transistor geometries were chosen to maintain the lowest possible junction resistances, which is crucial in applying this type of cell to any situation where current densities varies widely; even minute amounts of ohmic enhancement to the characteristic voltage, ΔV_{BE} , can impair gain accuracy, gain law conformance, and signal-path linearity at a stroke. Performance erosion due to secondary-tier transistor issues—including less-commonly considered basic parameters, weak avalanche, self-heating, and others—was explored during the design, using a specially-prepared CAD library that allows individual parameters to be selectively included or omitted. This valuable insight-generating hypothesis/test approach to simulation is called Foundation Design.

The input voltage, V_{IN} , is immediately converted to current form, V_{IN} / R_I , by the two resistors $R_I/2$. For this mode transformation to be accurately scaled and highly linear, the magnitude of the error voltage V_E —in both its linear and nonlinear component parts—should be much less than V_{IN} . This requires that the loop amplifier $A(s)$ has high voltage-gain and current-gain, under

all operating conditions. The high voltage gain ensures that the ΔV_{BE} is attenuated to insignificance; high current gain prevents diversion of signal current away from the collectors of Q_1 and Q_2 . This is a very challenging objective at maximum gain, when V_{IN} / R_I and I_D are smallest, and at high signal frequencies.

For example, with a typical full-scale ΔV_{BE} of 50 mV, and a minimum V_{IN} of 5 mV, then, in order to reduce V_E to $5 \mu V$ (that is, 0.1% of V_{IN}) the voltage gain $A(s)$ must be 10,000. This may sound like a reasonable value for the “open-loop gain” of a generic op amp. However, for a 100 MHz signal it demands a gain-bandwidth product $A(s)$ of 1000 GHz.¹⁷ A primary objective was to maintain a *perfectly constant* magnitude and phase response in the signal path, whether altered by V_G or V_M , for a specified total gain span of 100 dB. Figure 14 shows the *actual* gain and the remarkably stable AC response over a 105-dB gain span, achieved by varying V_G and V_M in combination so as to provide 22 *demanded* gain values at 5 dB intervals. In this study, the HF compensation networks were set for a higher bandwidth (230 MHz) than the more conservative center value (150 MHz) used for the production part. The package impedances were also omitted here, since the primary objective was to confirm the theory (see below), free of secondary confusing effects.

This extreme constancy in the AC response of a VGA is unprecedented. It is not unusual in extant products to see a “focal zone” at some high frequency in which the actual gain magnitude is almost completely independent of the demanded gain. This

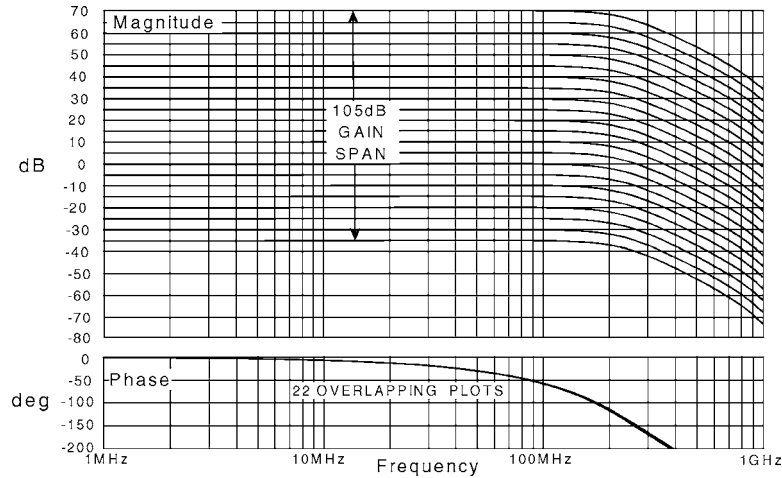


Fig. 14. AC gain and phase response of high-performance translinear VGA.

shortcoming is due to a variety of HF feed-forward sneak paths, that generate a larger output magnitude than the primary path; such effects also badly damage a linear phase response. During this design, all AC responses were routinely normalized to the 1 MHz value to examine the *relative deviation* at each gain setting (see lower panel of Fig. 14). An arbitrary design objective of ± 0.05 dB at 100 MHz was posed, and met, during the development. This insight-rich rigor is recommended in every VGA development, as a tool to explore fine-scale response anomalies.

This solution stems from first recognizing that the transconductance of the Q1/Q2 pair, g_{mD} , proportional to I_D , varies by 1000:1 over a 60-dB gain span. The input stage of the loop amplifier is a differential pair with a transconductance g_{mA} , proportional to I_A ; an on-chip capacitor C_F sets its *local* unity gain frequency to g_{mA}/C_F . But the feedback factor from its output back to its input is $g_{mD}R_I$, which likewise varies by 1000:1. To achieve a constant overall bandwidth, the product $g_{mD}g_{mA}$ is stabilized by arranging the tail current I_A to vary *inversely* as I_D . This is easily accomplished, since I_D is of the form $I_O \exp(-V_G/V_T)$, in the increasing-gain mode. By providing an accurately tracking inverse exponential current $I_A = I_O \exp(V_G/V_T)$, the overall unity-gain frequency is $g_{mD}g_{mA}R_I/C_F$, and since $\exp(-V_G/V_T) \cdot \exp(V_G/V_T) = 1$, it is constant. In the “gain down” mode, the exponentials are reversed. Incidentally, the form of I_D and I_A provide another example of *free mode* principles, where I_O and V_G play an equally vital role.

Thus, the overall -3 dB frequency is controlled directly by the accurate temperature stable (thin-film) resistors forming R_I and the half-sections of C_F (MOM capacitors) multiplied by the gain-independent ratio $I_D I_A / I_O^2$. These tail currents vary from about $4 \mu\text{A}$ to 4 mA, providing 5 dB overlap at each end of the gain range. The RTI voltage noise at full gain is ~ 5 nV/ $\sqrt{\text{Hz}}$, which is little more than the noise of R_I alone (4.02 nV/ $\sqrt{\text{Hz}}$, using $R_I = 1$ k Ω). The current-mode outputs, whose magnitude can be varied linearly by I_N over a further >40 -dB range, are applied to a pair of TZAs (wide-band transimpedance amplifiers), each with $Z_T = R_O/2$, and converted to balanced voltage-mode form, behind a well-controlled output impedance of 75 Ω per side. Their common-mode voltage level defaults to $V_S/2$, but can optionally be set by the user using a unity-scaled override. Figure 15 shows the measured RTI noise, with the input terminals (V_{IN}) short-circuited, at three temperatures. Figure 16 shows the main gain versus V_G in both the “Gain Up” and “Gain Down” modes, and the measured deviation (“gain linearity”), at three temperatures.

This forum does not allow a full discussion of many details and trade-offs in the design of this advanced VGA structure. Nevertheless, it serves to illustrate how, starting once again with the same 40-year-old current-mode core, the elaboration provided by a mixed bag of *free mode* principles transforms it from just an interesting *cell idea* to a powerful and versatile *product*, now in full production. Numerous such elaborations of rudimentary cores have generated an extended and still-growing family of such products. However, it would not

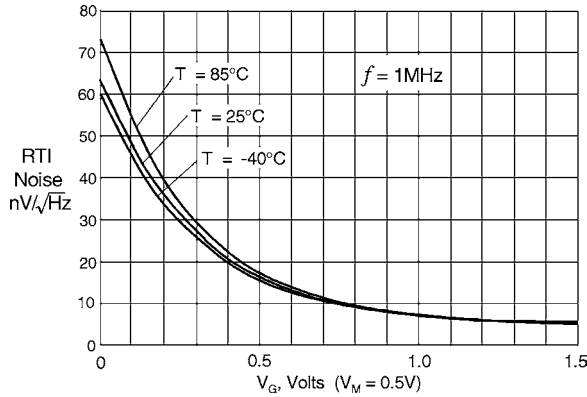


Fig. 15. Measured RTI noise spectral density vs. V_G at three temperatures.

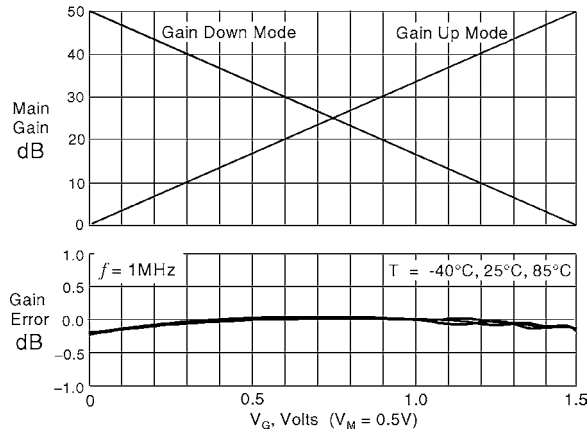


Fig. 16. Measured gain-up and -down and gain error vs. V_G at three temperatures.

be helpful to present these as “current-mode circuits”; indeed, the papers that described some of these developments never used that term in their titles.

4. Concluding Reflections

Science and engineering are deservedly well-regarded for their precision of expression. Rapid reference to numerous topics in our communication of ideas requires the ongoing development of a taxonomy, an agreed system of classification. This process is fueled by the widespread observance of its specialist terms over a substantial period of time, and eventually formalized by an institution such as the IEEE. The boundaries built into our pre-ratified taxonomy of integrated circuit design must be definitive, and its terms should be

both *appropriate* (as mind-joggers) and *unambiguous*, if they are to be of value as a tool of communication. But however carefully selected, coined and partitioned, the names we give to our topologies, techniques and tricks retain their importance as the vectors of essential ideas only if applied *carefully* and *frugally*, with full respect for the benefits of consensus. Such rigor is not routinely evident in the broad field of circuit design, and many cases of the misuse of inadequately-defined terms could be cited.

This paper offers an overdue clarification of the meaning of the term *current mode*, and proposes a Working Definition and Five Criteria that a circuit should exemplify in order to qualify. It is recommended that this useful, but narrow and specialized term, should be applied in an appropriately exacting manner. The Criteria should be used to test concepts that might, on first impulse, be referred to as “current mode” in nature. In view of the fact that their state variables are an even mix of currents and voltages, many of the circuits published in recent years cannot properly employ this term. It is surely in the interest of authors, and the community at large, that paper titles and key words capture the essential and specific *top-level* features of each advance in circuit design. This rigor will set the stage for the subject, and provide the busy reader (all of us) with a clearer pre-view of both the context and the content. It will also facilitate searches, and reduce the number of false positives, the bane of filtering the ever-expanding warehouse of technical literature.

It was noted that the fastidious management of the *voltage-current product*—the signal *power*—is often a designer’s primary concern. The term *impedance-mode* might be used in this domain, since the circuit techniques are dominated by considerations of source-load matching and the maximization of power transfer. However, the value of introducing yet another class into an already-bulging taxonomy is debatable. Similarly, little would be gained by referring to charge-coupled devices or switched-capacitor circuits by using the term *charge mode* to draw attention to their exploitation of this particular state variable. For so-called “current-mode logic” (CML), the term *g_m mode* might be more appropriate in the quest for precision, since its state variables are in fact entirely in *voltage mode*. But here, the preferred and well-established term *current-steering* clearly defines this logic family; and unlike *emitter-coupled logic*, it is technology-blind.

Signals in analog circuits are universally characterized by frequent *mode transformations*. Product

designers are obliged to adopt a fluid viewpoint, as each sub-region is developed. Since the term *mixed mode* is widely understood to refer to integrated systems in which analog and digital signals co-exist, the term *free mode* is proposed. It is emphasized that this term is not intended to be used to define, distinguish or name a class. It simply refers to an appropriate *perspective* on design, useful as a *mnemonic*. Thus, since all oscillators, filters, pulse-shaping, delaying, timing and rate functions (integration and differentiation) are necessarily free mode in form, there would be no point or purpose in titling a paper, for example, “A *Free-Mode Voltage-to-Frequency Converter*”; they all are!

This paper’s frequent emphasis on *practical value* should not imply a lack of respect for formal theories, or the pursuit of insight-generating algebraic analyses (even though these often require falling back on approximations). Rather, it stems from the concerned observation that many papers and letters published about a variety of small-cell notions suggest a very limited view of the broader sweep and practical needs of today’s IC industry. The merits of another incremental reconfiguration of familiar cell topology are often hard to identify. In practicing design with the purpose of solving pressing contemporary problems, and satisfying specific and difficult real-world needs, we must keep in mind that the generic circuit fragments and tricks, that we designers amass in our portfolios over time, are for the most part servants-in-waiting, for future and adaptation and deployment in meeting a variety of practical objectives. Unless and until they are developed into complete, robust products that are able to address increasingly-stringent real-world demands, cells remain of little value, except as mental stimulants and didactic tools.

Our technologies have always had their greatest significance and influence when applied within the context of everyday life. Very often, their latent values lie in reserve for years, waiting to be understood and appreciated, and then imaginatively exploited through the inventive efforts of the community of pragmatic and resourceful product designers. We must each be *self-challenged* to pursue genuine novelty, and seek to transform our personal bag of tricks, assorted and many-modal, into the affordable and reliable products that will rapidly leave our realm of the intriguing and arcane, to take their place with all the other modern indispensable commodities, and become unremarkably commonplace.

Notes

1. A super-conducting ring might be classified as a “pure current-mode” device, since current is sustained without an associated voltage drop. Such a totally-closed loop cannot meaningfully be called a “circuit”.
2. Current-mode input or output interfaces are sometimes required by the application. Thus, a logarithmic amplifier in fiber-optic power-measurement systems must accept its input as a current from a photodiode.
3. More generally, a polynomial of the form $f = f_0 + \{(V_{IN}/V_R) \pm b(V_{IN}/V_R)^2 \pm c(V_{IN}/V_R)^3 \dots\} f_S$.
4. “The development of analog cells is 70% bias design and 30% signal-path design”. This lecture-room maxim is obviously a generalization. Nevertheless, the design of the core function of an analog circuit is usually straightforward, while the provision of robust and artifact-free biasing requires careful thought.
5. The ratio of the largest permissible signal to the noise floor, both defined as RMS quantities for a stated bandwidth, is commonly referred to as “dynamic range” and specified in decibels. However, this term needs to be carefully defined within a particular context, since many interpretations can apply.
6. In the examples in this paper, the assumed operating temperature is 300 K, unless otherwise stated.
7. While V_{BE} offset voltages are PTAT, they are partly a manifestation of fixed, non-unity emitter-area ratios. Such mismatches cause a variety of temperature-invariant errors in current-mode cells.
8. When first used, colleagues called this general form a GCM (Gilbert Current Mirror). The author prefers cell names that define structure. Note that, simply as a useful mnemonic, the figure superimposes a “V”.
9. A finite source resistance r_{SRC} transforms to $-r_{SRC}$ at the output. However, when used as a *differential current balance* the r_{SRC} due to the V_{AF} of the two sources cancel at $I_1 = I_2$ when these currents are balanced by an outer feedback loop. Thus, as a control-loop integrator, the final error is very small.
10. Exemplifying this criterion, the first paper on current-mode amplifiers and multipliers in the Journal of Solid State Circuits was also the first to be cited 100 times in later papers. While the current mirror was the *first current-mode cell* of notable and enduring value, this term was not in general use at that time.
11. CMOS transistors for use in “inverter-style” logic required them to be enhancement-mode types, giving the current mirror a new lease of life when CMOS was turned to analog applications.
12. In cases where this gain or loss factor must be robust in production, integer emitter units would be used. The ratio M could, of course, differ for the two mirrors.
13. But this is not always the case, as discussed in the paper *Distortion Due To Self-Heating In Translinear Multipliers Using Thermally-Isolated Bipolar Transistors*, to be published at a later date.
14. While this is essentially correct, slight increases in the characteristic voltage caused by the device’s contacting resistances corrupt the purity of Eq. (2) even in this basic current-mode cell. These voltage-mode aspects of the cell’s internal behavior demand careful consideration in many practical applications,

particularly when the current densities must be high in order to minimize the effective inertia of the cell.

15. For an interesting elaboration of the Fig. 8(b) form, see the Data Sheet for the Analog Devices AD538.
16. This form differs from that of an ideal differential pair, which would show a reduction of gain of 0.117 dB at ± 6 mV ($T = 25^\circ\text{C}$). The actual form is modified by the choice of biasing and device scaling.
17. GBW products much higher than this ($>50,000$ GHz) are routinely achieved in RF logarithmic amplifiers; but these use many cascaded stages without feedback. Here, we have a feedback system containing two g_m stages. The detailed design of the voltage-mode amplifier A(s) is the key to this successful implementation.

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