

# Scalable Front-End Digital Signal Processing for a Phased Array Radar Demonstrator

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**Abstract**—The European Space Agency (ESA) is in the process to develop a ground-based space surveillance radar for its involvement in the Space Situational Awareness (SSA) Preparatory Programme [1]. The radar is intended to systematically survey and track all objects above an altitude dependant size threshold in the low Earth orbit and, based on these data, maintain a catalogue with physical and orbital information. Phased array radar demonstrators are currently being developed by industry in cooperation with ESA. These radars are precursor systems and will assist in the definition of the final SSA radar architecture. In support of these developments a small-scale phased array radar demonstrator is being developed at the European Space Operations Centre (ESOC). The system is not intended to detect space debris objects but to implement the general functionality of its large-scale counterparts. This paper describes the mini-radar design and implementation. Furthermore, measurement results showing the performance of the system are presented. In order to cope with the high data processing throughput demand at the multi-channel receiver, an efficient field-programmable gate array (FPGA) implementation is adopted for the front-end pre-processing and digital beam-forming. As the computational burden for the forthcoming SSA phased array radar architecture including several hundreds or thousands of receiver elements is very high, an estimation of computational complexity for different signal processing building blocks is presented here.

**Keywords:** *space situational awareness, phased array radar; digital beam-forming; FPGA*

## I. INTRODUCTION

The mini-radar demonstrator described here is based on previous work described in [2] and is intended to serve as an internal cross verification for the on-going radar breadboard developments contracted to industry within the framework of the Space Situational Awareness (SSA) Preparatory Programme. The system is envisaged to be flexible enough to implement different radar concepts, such as bi-static as well as close mono-static radar systems. The system design of the mini-radar includes one transmitter and one receiver rack. Both racks are mobile so that measurements at different locations can easily be performed. Waveform flexibility is achieved with an arbitrary waveform generator included in the transmitter rack. It is foreseen to focus on two waveforms which were identified in earlier studies [3], being Continuous Wave (CW) and pulsed Linear Frequency Modulation (LFM). The

transmitted radar signal is centered at 1307 MHz and has a maximum transmit power of 10 W. Both transmitter and receiver are equipped with a planar 16-element array antenna. Transmit beam-steering in azimuth and elevation is achieved by means of digitally controlled phase shifters in the 16 transmitter branches. The receive antenna array is followed by 16 fully parallel receiver chains. In each chain the signal is amplified, filtered, down-converted, analog-to-digital (A/D) converted and then processed by a field-programmable gate array (FPGA) application and a subsequent general purpose computer. In order to cope with the high input data rate of 9.6 Gbit/s, the full front-end signal processing and digital beam-forming is implemented in the FPGA. The use of FPGAs allows for high processing throughput, and provides the flexibility to change the processing application enabling the support of different radar waveforms.

Several recent research projects have used FPGAs to implement digital beam-forming in receiving array systems. In [4], a Xilinx Virtex 5 FPGA in combination with a multi-channel A/D converter is used to form a single beam from 8 receive channels. More recently, a phased array radar receiver including channel pre-processing and beam-forming for 64 channels has been developed based on an Altera Cyclone III device in [5]. The flexibility of the receiver is demonstrated by means of two radar applications, a weather radar using 3 MHz signal bandwidth while synthesizing 24 parallel beams, and an aircraft tracking radar using 12 MHz signal bandwidth and forming 6 beams. In [6], a K-band radar is described consisting of 8 transmitter and 8 receiver elements. The FPGA application for system control and signal processing is split into time critical operations handled by direct hardware and non time critical operations handled by a soft-core microprocessor embedded in the FPGA design.

In a large scale phased array radar, such as the forthcoming SSA radar including several hundreds or thousands receiving elements, the high front-end processing load is often distributed throughout a network of processing nodes implementing the front-end processing for a single receive channel or combining several channels in one node. The processing capacity of a single node thereby plays a critical role for design of the entire network. Rather than fixing a specific design point, this paper is concerned with the estimation of computational complexity in terms of FPGA resource utilization for different signal processing building blocks and different parameters, such as

the number of input channels, the number of synthesized beams and the signal bandwidth. Section II of this paper describes the mini-radar system design and explains the signal processing architecture in the receiver. Corresponding measurements are provided in Section III. Synthesis results of the FPGA implementation are given in Section IV. Section V shows tests of the full radar system and Section VI concludes the paper.

## II. MINI-RADAR DESIGN

The design goal of the mini-radar demonstrator is to implement a flexible, low-cost radar system. To fulfill the cost constraint, the design was restricted to use mostly inexpensive mass-market products. This led in some areas to a design which deviates from the optimum approach. Nevertheless, these deviations only have a minor effect on the radar functionality and performance. Fig. 1 shows a high-level diagram of the mini-radar system.

### A. Transmitter design

The radar transmitter consists of an arbitrary waveform generator, capable of generating the two waveforms to be studied within the project: CW and LFM. The CW signal is intended for a bi-static radar configuration, whereas the pulsed LFM signal will be used in a (close) mono-static configuration. The radio frequency (RF) signal delivered by the signal generator is distributed onto 16 transmit chains each of which includes a 6-bit 360° digitally controlled phase shifter and a power amplifier of 33 dB gain and 1 W output power. The power amplifier is followed by a low-pass filter to prevent the transmission of harmonics. The radar antennas designed within the frame of this project are microstrip planar arrays. The transmit antenna is a 4 by 4 patch array antenna on a single hydrocarbon ceramic substrate, which is characterized by dual coaxial-fed square elements and supports horizontal and vertical polarization.

### B. Receiver Design

The mini-radar receive antenna is a 4 by 4 dual layer antenna array. As in the transmitter, the substrates are RF hydrocarbon ceramic laminates and the elements are fed by dual coaxial probes. The antenna is followed by the analog

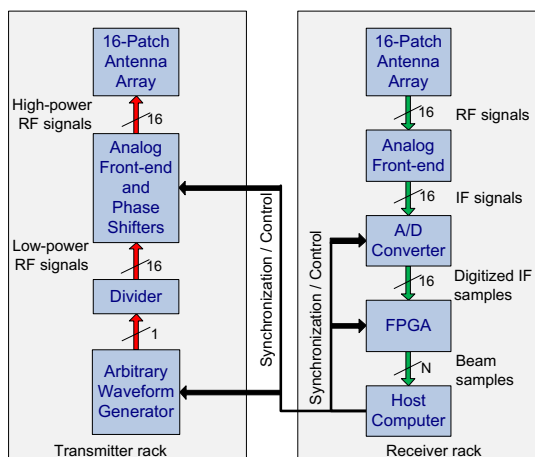


Figure 1. High-level diagram of the mini-radar system design

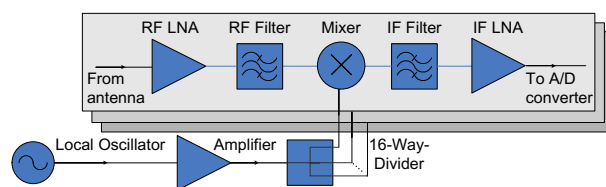


Figure 2. Receiver analog front-end design

front-end, in which the RF signals are amplified, bandpass-filtered, and down-converted. The analog front-end provides at its output a bandpass signal at an intermediate frequency (IF) for each individual chain. A block diagram of the receiver analog front-end is shown in Fig. 2.

In addition to requirements on noise figure, intermodulation performance, and dynamic range, design decisions for the analog receiver paths are driven by the requirements of the A/D converter as the received signals have to be conditioned for IF digitization. The A/D converter can simultaneously sample 32 channels at a rate of 50 MHz. The IF for bandpass digitization is set to 20 MHz. This IF brings the nearest image frequency that will spuriously be mixed to the receiver’s pass band relatively close the pass band edge, and thus a suitable image rejection filter must be employed prior to the down-conversion in order to protect the pass band. A second bandpass filter is used in the IF branch of the analog path to prevent spurious mixer outputs from aliasing into the pass band. The analog receiver paths require a minimum gain of 52 dB to “lift” the input signal into the dynamic range of the A/D converter and minimize the system signal-to-noise ratio (SNR) degradation by quantization noise generated during the A/D conversion process. This gain is achieved by two low-noise amplifiers (LNAs) in combination with a built-in variable-gain amplifier in the A/D converter card.

The radar system is controlled from the host computer integrated in the receiver rack which sets the configuration of the A/D converter and FPGA application in the receiver. Furthermore, it issues write commands to the digitally controlled phase shifters in the transmitter rack in order to perform transmit beam-forming, and it issues a trigger signal to execute a radar pulse transmission. The pulse trigger is synchronized to the FPGA master clock and is received by both the transmit signal generator and the FPGA to indicate the beginning of a transmit/receive window. All local oscillators and clocks in the system are synchronized through a common reference clock signal to ensure coherent operation. The cables carrying the synchronization and control signals have a length of 100 m in order to allow for sufficient spatial separation between the two racks.

### C. Receiver Signal Processing Architecture

The A/D converter delivers the 16 parallel channel samples with 12 bit precision at a sampling rate of 50 MHz resulting in a data rate of 9.6 Gbit/s. Therefore, the front-end signal processing is implemented in the FPGA in order to satisfy the throughput demand for real-time processing and the timing requirements (clock-synchronous pulse trigger). Fig. 3 shows the signal processing architecture and the corresponding FPGA implementation. The IF signals of the 16 channels are

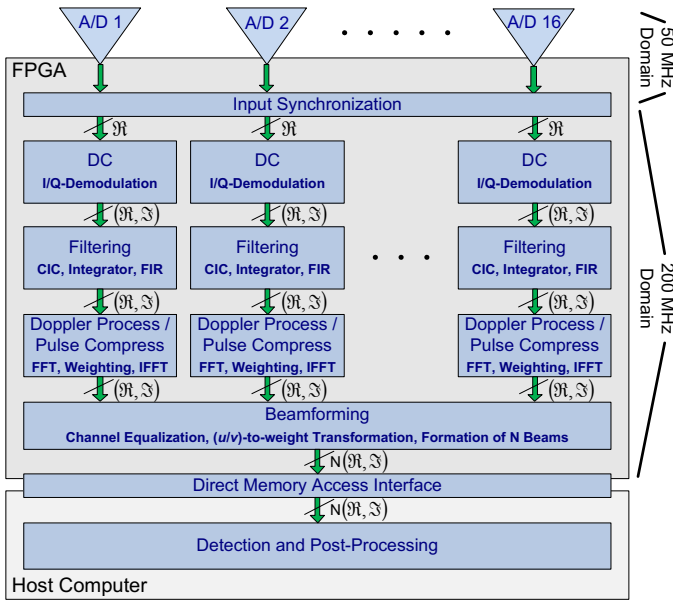


Figure 3. Receiver signal processing architecture

converted to complex baseband in the down-converter (DC) stage using direct digital synthesis (DDS) to generate the demodulation signals. Subsequent band isolation and decimation is performed by cascaded integrate-comb (CIC) and/or finite impulse response (FIR) filters. The parameters of the filtering stage depend on the signal waveform used. In the case of CW radar operation, the signal bandwidth only incorporates the carrier and the range of expected Doppler shifts. A typical value for the maximum expected frequency shift for space debris objects in the low Earth region is  $\pm 75\text{kHz}$ . Hence, the pass band of the filtering stage should be very narrow and the sample rate reduction can be very high. An LFM baseband signal, on the other hand, usually has significantly larger bandwidth. The filter bank therefore requires a wide pass band and performs only moderate sample rate reduction. The reconfigurability of the FPGA enables seamless switching between the two operational modes.

The following processing stages perform transformations on the incoming data stream, likewise different for each operational mode. The incoming data flow of complex baseband samples is considered as a 3-dimensional data cube consisting of one spatial and two temporal dimensions: the

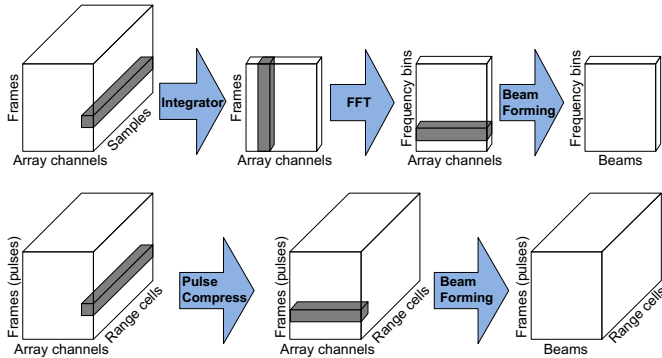


Figure 4. Data cube transformations performed in the FPGA application for CW (top) and LFM (bottom) operation. The dimension that is operated on in one processing step is indicated by a shaded bar.

range cell or fast time dimension corresponding to the sampling interval and the frames dimension corresponding to the frame (or pulse) repetition interval. The subsequent data cube transformations for CW and LFM operation are shown in Fig. 4. Since a CW signal does not exhibit any range information, this dimension is eliminated in the CW case by integrating all samples within a frame repetition interval. The time domain data is then transformed into frequency domain performing a Fast Fourier Transform (FFT) over the frame repetition interval in order to obtain the spectrum of Doppler frequencies. Finally, the spatial dimension of array channels is transformed into beams by the digital beam-former. In the LFM case, the baseband signals are first submitted to the pulse compressor. The pulse compression is implemented by means of a fast convolution using FFT and inverse FFT (IFFT) pairs and multiplication of a reference waveform in the frequency domain. After the pulse compression, the beam-forming is performed as the last transformation step. The FPGA LFM application does not perform pulse-to-pulse processing which is left to the host computer.

In the beam-former, multiple beam-forming coefficients sets are applied to the same set of baseband samples in order to create multiple beams. The beam-steering information is stored in an FPGA-internal table which is loaded via the host computer. In order to calibrate the receiver and to eliminate unwanted phase and amplitude differences between channels caused by imperfections of the analog front-end, a set of complex equalization coefficients is provided by the host computer. Typical parameters of a CW and an LFM application are shown in Table I.

The sampling rate reduction as a result of decimation entails a reduced computational burden in subsequent stages, which is exploited to apply extensive hardware folding, i.e. logically

TABLE I. PARAMETERS FOR THE CW AND LFM APPLICATION

CW configuration		
Down-conversion	DDS frequency resolution	0.0233 Hz
	DDS spurious-free dynamic range	102 dB
Filtering	CIC stages	4
	CIC decimation ratio	128
	Integration steps	4
	FIR high-pass filter order	78
Doppler processing	Output sample rate	97.7 kHz
	FFT size	1024
Beam-forming	FFT windowing	Hann
	Number of synthesized beams per frame repetition interval	256
LFM configuration		
Down-conversion	DDS frequency resolution	0.0233 Hz
	DDS spurious-free dynamic range	102 dB
Filtering	FIR low-pass filter order	38
	Decimation after FIR filter	7
	Output sample rate	7.1 MHz
Pulse compression	Pulse length (uncompressed)	500 $\mu\text{s}$
	Pulse bandwidth	6 MHz
	FFT / IFFT size	4096
	Reference waveform weighting	Taylor (-40 dB side lobe level)
Beam-forming	Number of synthesized beams per frame repetition interval	256

parallel operations can be performed in a time-multiplexed fashion making reuse of hardware and avoiding its physical duplication. Besides hardware folding enabled by sample rate reduction throughout the processing chain, a second possibility of hardware folding arises from the fact that the FPGA generally can be clocked at frequencies higher than the A/D converter sampling clock of 50 MHz. Since a fully parallel implementation of the processing for all 16 channels would either way exceed the FPGA resources, the channel samples are serialized into sub-groups of  $L_{TDM} = 4$  time division multiplex (TDM) channels which are subsequently processed in a time-multiplexed fashion at a clock rate that is 4 times higher than the sampling rate of 50 MHz. This greatly reduces the FPGA resources required by this architecture. The 200 MHz clock is internally derived from the sampling clock by a built-in digital clock management (DCM) tile.

The host computer acquires the beam samples from the FPGA. The samples are transferred to the host computer via direct memory access (DMA). The host computer performs different back-end tasks, such as the calculation of channels equalization coefficients, constant-false-alarm-rate (CFAR) detection or data logging.

### III. RECEIVER SIGNAL PROCESSING MEASUREMENTS

The receiver signal processing application with the parameters given in Table I for CW and LFM operation has been validated in laboratory tests. Fig. 5 shows the FPGA output data after injection of a CW signal and a compressed LFM pulse, respectively, into the analog receiver front-end. The beam-forming coefficients have been set to split an azimuthal sweep from -90 to +90 degrees into the 256 parallel beams.

The system processing gain in terms of SNR improvement throughout the different processing stages has been measured

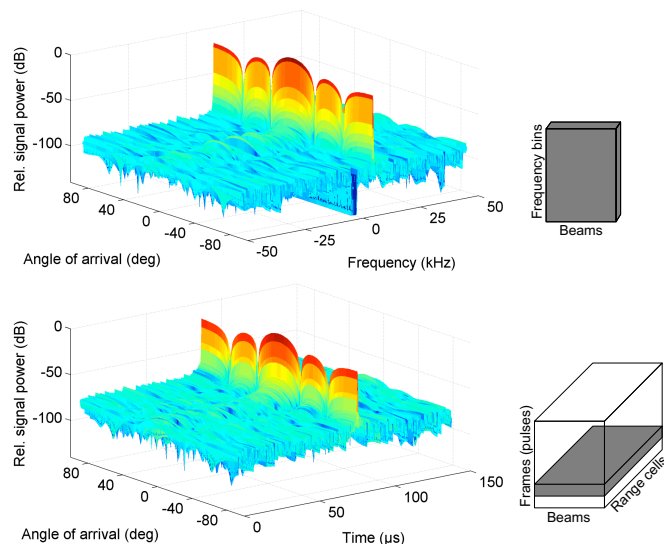


Figure 5. Processed data cube for a CW signal with 8 kHz frequency offset (top) and a slice of the data cube for one delayed LFM pulse (bottom). All array channels are fed with zero phase difference corresponding to a wave impinging from boresight. The beam-forming pattern in azimuth thus maximizes the signal power at an angle of arrival of zero degrees.

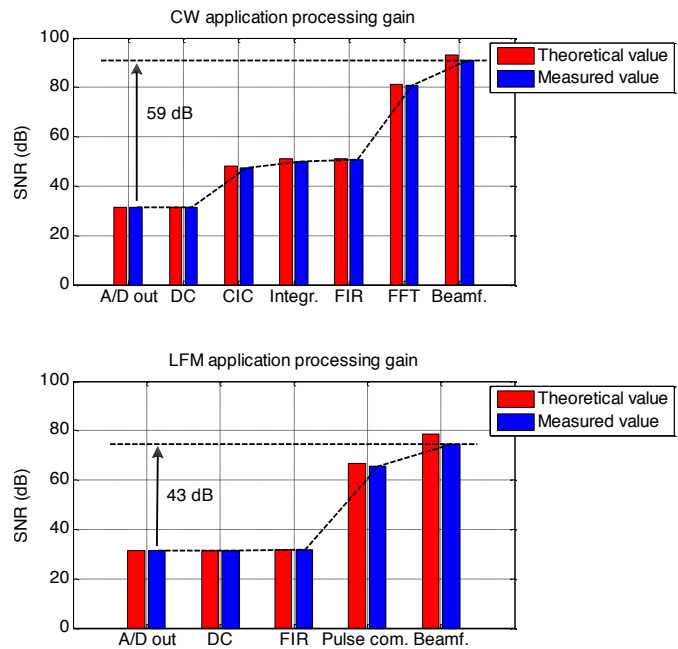


Figure 6. SNR values measured at the output of each processing stage of the CW (top) and the LFM (bottom) application

and compared against the theoretically expected value as shown in Fig. 6. The largest deviation of around 2.5 dB from the theoretical value is observed in the beam-former. This deviation from the optimum comes from the fact that the phase noise generated by the local oscillator in the analog front-end constitutes a noise source which is common to all receive channels. This noise contribution therefore is not completely uncorrelated throughout the channels and benefits from the beam-forming gain in the same way as the signal. An oscillator with improved phase noise performance has been found to solve the problem. This option, however, has been discarded due to budgetary constraints and the 2.5 dB deviation is tolerated.

### IV. SYNTHESIS RESULTS

The FPGA used in this project is a single Xilinx Virtex 5 FPGA (XC5VSX50T). The FPGA implementation has been verified and synthesized using the Xilinx ISE 10.1 tool chain. In the following, synthesis results are shown for varying throughput, number of input channels, and input signal bandwidth. The computational complexity of the signal processing task is thereby expressed by FPGA resource utilization, i.e. the consumption of lookup table (LUT) and register (REG) resources, embedded digital signal processing (DSP) slices containing a hard-wired multiplier and adder logic, and block random access memory (BRAM) slices. All results are taken from fully placed and routed FPGA designs. The sampling clock rate is fixed to 50 MHz and the maximum processing clock is set to 200 MHz ( $L_{TDM} = 4$ ). Although higher clock speeds can be achieved with the Virtex 5 FPGA, this value was found to be a reasonable upper limit when the resource utilization increases. It has been ensured during synthesis that all designs meet these timing constraints. The synthesis results for the two design points in Table I for 16

## V. RADAR SYSTEM TESTS

TABLE II. FPGA RESOURCE UTILIZATION FOR THE CW AND LFM APPLICATION IN TABLE I (16 RECEIVE CHANNELS)

Application	CW	LFM
REG utilization	13100 (40%)	9864 (30%)
LUT utilization	6664 (20%)	7639 (23%)
BRAM utilization	49 (37%)	55 (42%)
DSP utilization	126 (44%)	134 (47%)
Execution time		
CW: 1024 frames x 256 beams	16.8 ms	23.7 ms
LFM: 4096 range cells x 256 beams		
Computational load	11.2 GOPS	15.7 GOPS

array channels are listed in Table II. Given the parameters in Table I, the execution time is the time needed to process the complete reduced data cube (CW) or a slice of the data cube for one pulse (LFM). The computational load for this task is measured in billion operations per second (GOPS), while one operation is either a real addition or a real multiplication.

The FPGA resource utilization remains invariant for a varying number of beams. Increasing the number of beams, however, requires a longer processing time since the beams are formed sequentially from one set of channel samples. The execution time is composed of three contributors: the time to acquire, down-convert and filter the required amount of samples, the time to perform Doppler processing or pulse compression, and the time required for beam-forming. The latter can be easily reduced by increasing the parallelism degree of the computational units in the beam-former. Fig. 7 shows the area-time (AT) trade-off for different parallelism degrees. The area consumption is thereby measured in the utilization of FPGA DSP slices which are found to be exhausted first in almost all synthesized designs. The results show that, for an increasing parallelism degree, the CW application becomes less efficient in terms of the AT product, while the LFM application becomes more efficient. Compared to the computational load for a parallelism degree of one in Table II, the workload for a parallelism degree of four is increased to 14.6 GOPS and 46.7 GOPS, respectively.

Fig. 8 and Fig. 9 show the resource utilization of the CW and LFM radar implementations for a varying number of receive channels and varying signal bandwidth while fixing beam-former parallelism degree to one and the remaining parameters according to Table I.

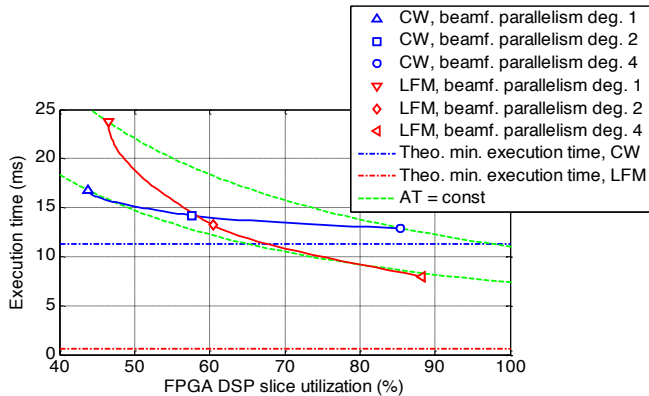


Figure 7. Area-time trade-off for different parallelism degrees of the computational units in the beam-former. The theoretical minimum execution times correspond to fully continuous data streaming. They are given by the output sampling frequency and the number of samples to be acquired.

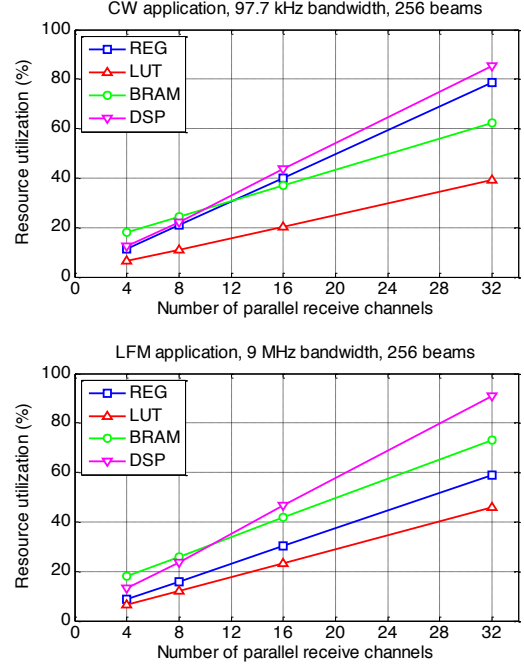


Figure 8. FPGA resource utilization of a CW (top) and an LFM (bottom) application for different numbers of receive channels

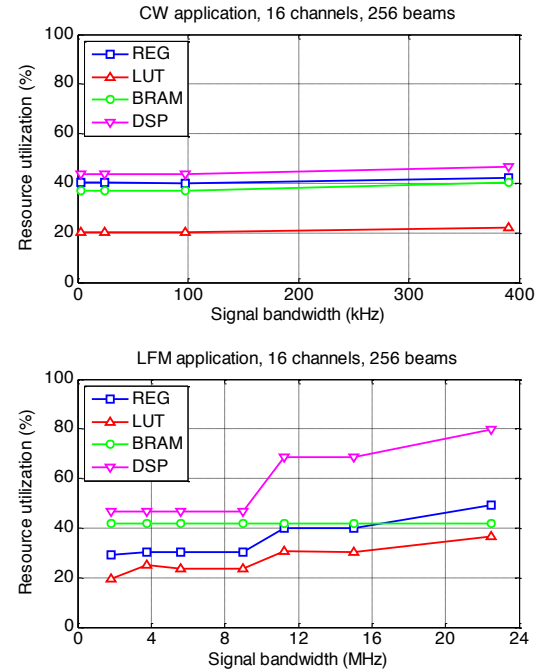


Figure 9. FPGA resource utilization of a CW (top) and an LFM (bottom) application for different signal bandwidths

CW radar tests have been performed to estimate the three target properties that can be directly measured with a CW radar: the angular displacement of the target in azimuth and elevation and the radial velocity with respect to the receiver. Transmitter and receiver have been placed in a close mono-static configuration as shown in Fig. 11. The target was a

person passing in front of the radar setup with varying walking speed. The Doppler frequency filtering sufficiently suppressed direct transmitter-receiver coupling and background reflections by means of the receiver's high-pass filter (see Fig. 5). The angle of arrival and radial velocity measurements reflect the diagonal two-way trajectory from left to right and vice versa. In a second measurement setup, the transmit beam has been continuously steered to 64 different beam pointing positions to perform surveillance of a field of view in the sky as shown in Fig. 12. The results show the detection of a target (bird) passing through the field of view. The output sample rate of the filtering stage has been reduced in both measurements to 0.8 kHz and 3 kHz and the transmit power to 100  $\mu$ W and 1 mW per channel, respectively. Table III shows a link budget calculation for the full-scale transmit power.

TABLE III. MINI-RADAR LINK BUDGET CALCULATION

System properties	Transmit power	40	dBm
	Min. required SNR	20	dB
Target properties	Reference radar cross section (metallic sphere with 0.5 m radius)	-1.1	dBm <sup>2</sup>
Antenna properties	Transmit antenna gain (no tapering)	16	dBi
	Receive antenna gain (single element)	6	dBi
Receiver noise	Receiver noise temperature at 1 <sup>st</sup> LNA input (290K physical temperature)	170.4	K
	Analog front-end noise bandwidth	8.8	MHz
System losses	Receiver cable and additional losses (due to implementation imperfections)	3.6	dB
<b>CW operation</b>			
Receiver processing gain		59	dB
Required signal level at 1st LNA input		-145.7	dBm
Reference range		8556	m
<b>LFM operation</b>			
Receiver processing gain		43	dB
Required signal level at 1st LNA input		-130.3	dBm
Reference range		3432	m

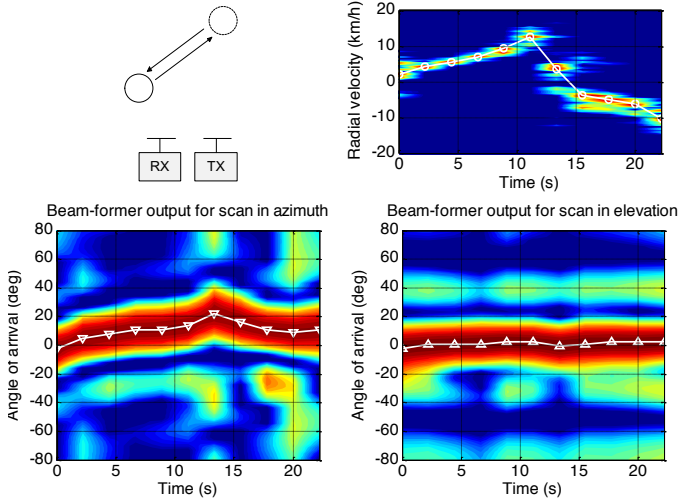


Figure 11. Radial velocity (top right) and direction finding (bottom) measurements with a person passing in front of the radar setup. Red colors correspond to high signal power, blue colors correspond to low signal power.

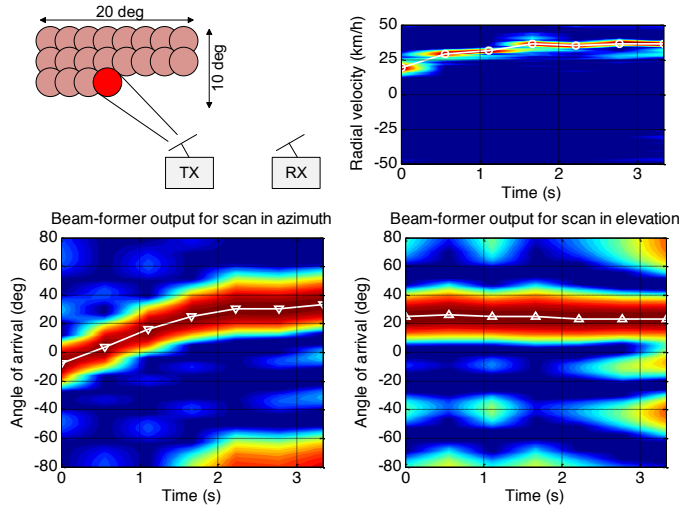


Figure 12. Radial velocity (top right) and direction finding (bottom) measurements for surveillance of a field of view in the sky (top left). Red colors correspond to high signal power, blue colors correspond to low signal power.

## VI. SUMMARY AND OUTLOOK

This paper describes the design of the ESA phased array mini-radar demonstrator, which is intended to serve as an experimental reference system for ESA's involvement in the SSA Preparatory Programme. Besides a system description, the FPGA application which implements the front-end signal processing in the receiver is presented in more detail. The two implementations for CW and LFM operation are scalable in the number of input channels, signal bandwidth, and the number of beams. The computational complexity imposed by the real-time channel pre-processing and digital beam-forming is estimated in terms of FPGA resource utilization. The processing capacity that is achievable with a single exemplary FPGA device is determined. Such implementation can be considered as a processing node in a larger scale phased array receiver in the context of a future SSA radar. Radar tests that demonstrate the performance of the receiver and the mini-radar system are presented. Future activities will focus on further signal processing techniques for LFM operation and long-range tests for both operational modes.

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