Scalable Front-End Digital Signal Processing for a Phased Array Radar Demonstrator

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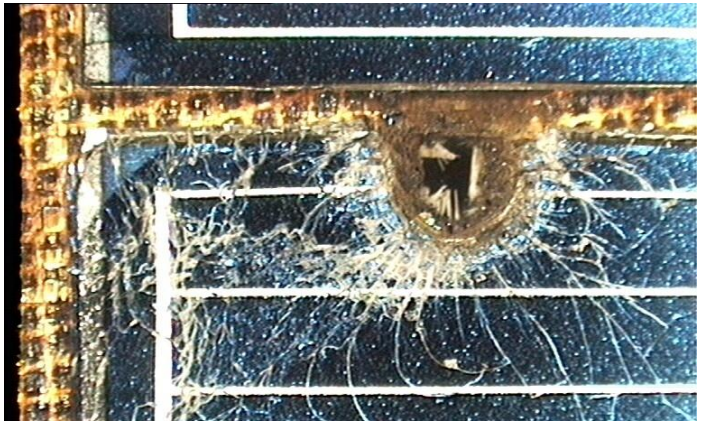
Background of the SSA activity

- Context
  - ESA Space Situational Awareness (SSA) initiative
- Objective of the SSA initiative
  - Support of the European independent utilisation of and access to space
- 3 segments
  - Space weather events
  - Near-Earth Objects: Potential asteroid impact hazards
  - Space Surveillance and Tracking: Objects orbiting the Earth

Impact on Hubble solar panel



Source: http://www.esa.int/ssa

SSA Radar Element

Managed by ESA and contracted to Industry

	2010 - 2012	2013 - 2020
Timeframe		
System	Phased array radar demonstrator →	Radar to catalogue objects in low-Earth orbit
Detection design goal	~ large objects	~5-10cm objects at 800 km altitude

ESA internal development

Independent experimental system in support of SSA Radar Element

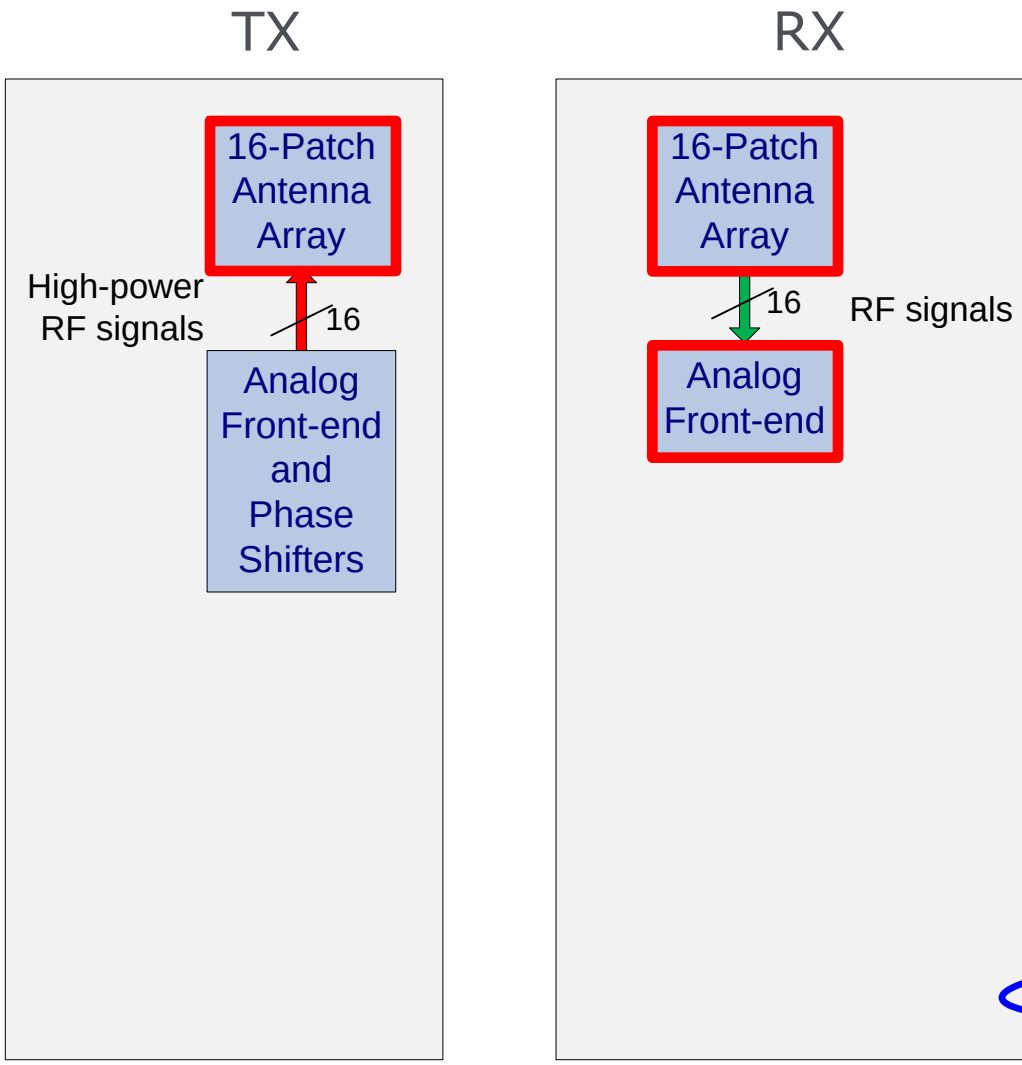
Mini-Radar demonstrator

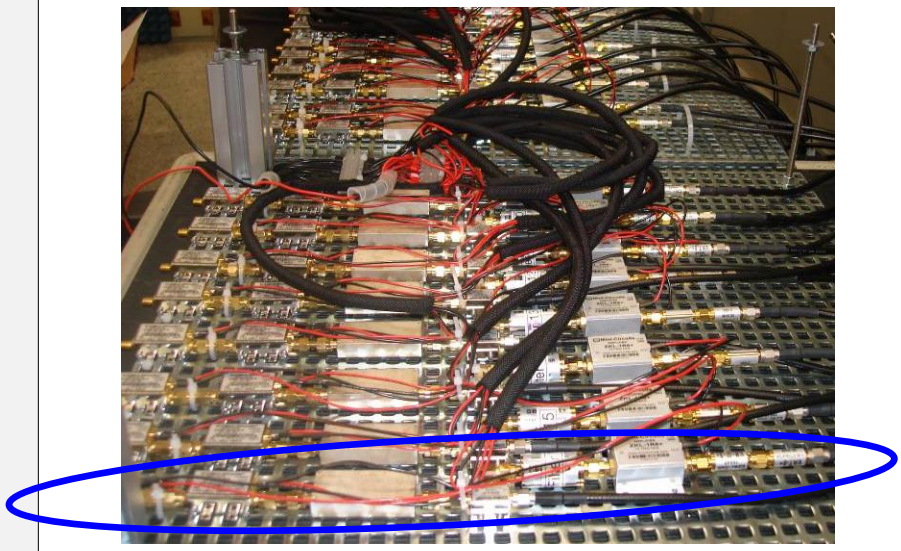
Not designed for space surveillance but for nearby objects

Outline of presentation

- Space surveillance for ESA's SSA preparatory programme
- Mini-Radar system architecture
- FPGA signal processing architecture
- Synthesis results
- System tests
- Summary and outlook

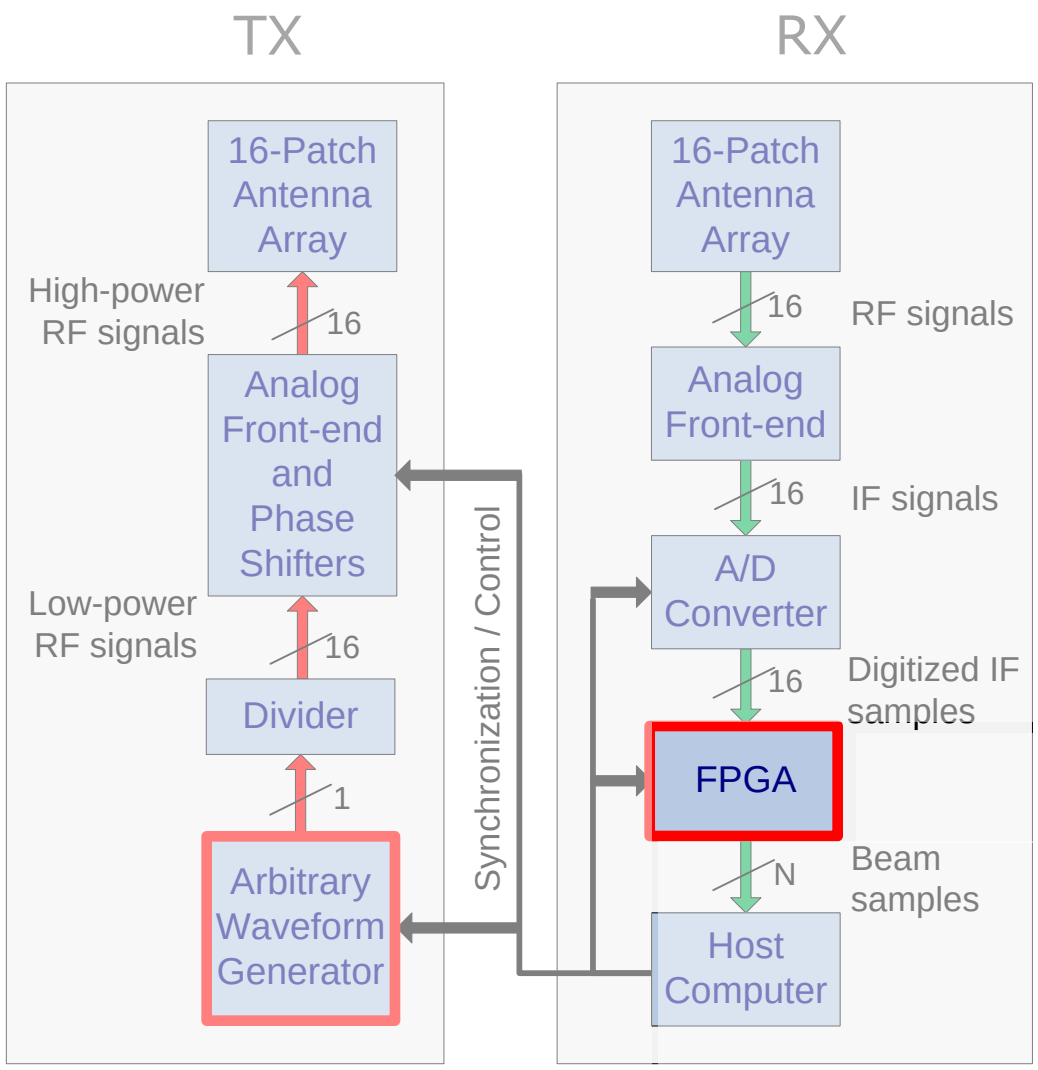
Mini-Radar System Architecture





16 fully parallel TX/RX chains

Mini-Radar System Architecture



- Waveform flexibility: CW or pulsed LFM
- Large-scale phased array radar:
  - Distributed processing nodes
  - Computational burden for a single node?
- Scope of this work:
  - Estimation of computational complexity wrt. FPGA utilization

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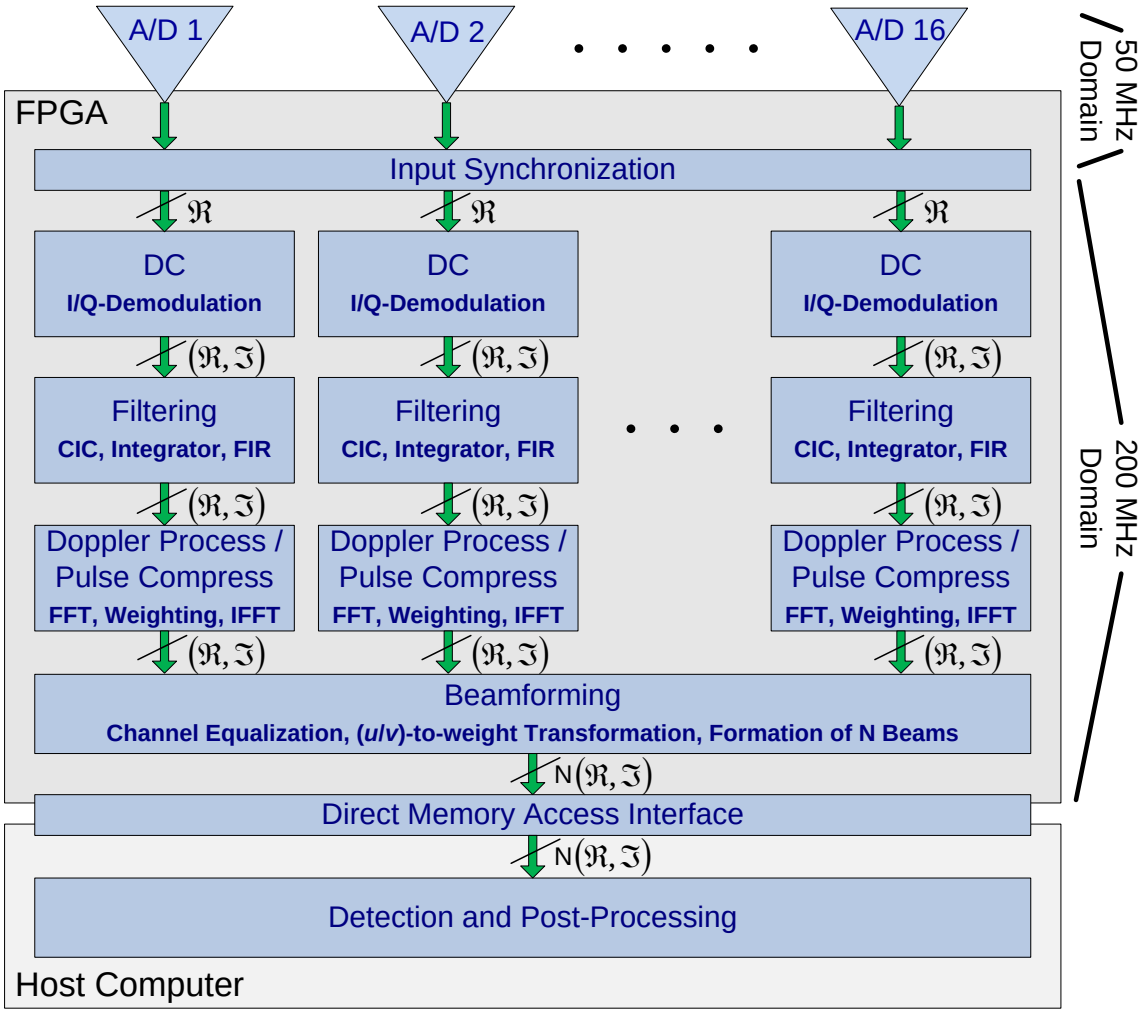
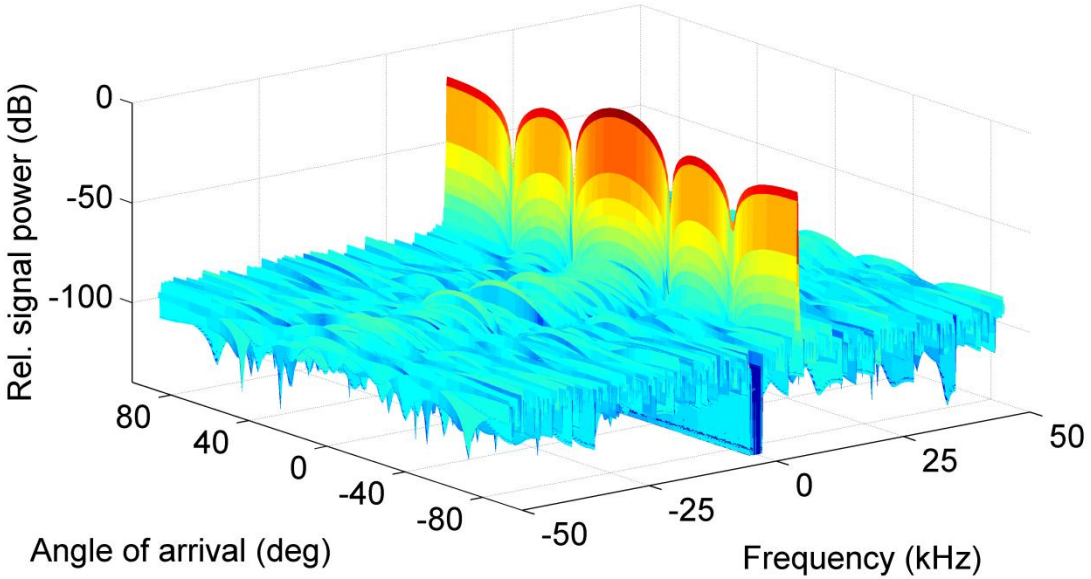
FPGA Signal Processing Architecture

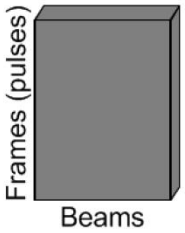


- Simultaneous sampling of 16 RX channels
- Digital down-conversion to complex baseband
- Low-pass filtering, high-pass filtering, integration
- FFT processing (CW) / Pulse compression (LFM)
- Channel equalization / Digital beamforming
- Transfer to host PC
- FPGA Implementation: Hardware-folding 4-to-1 to save FPGA resources

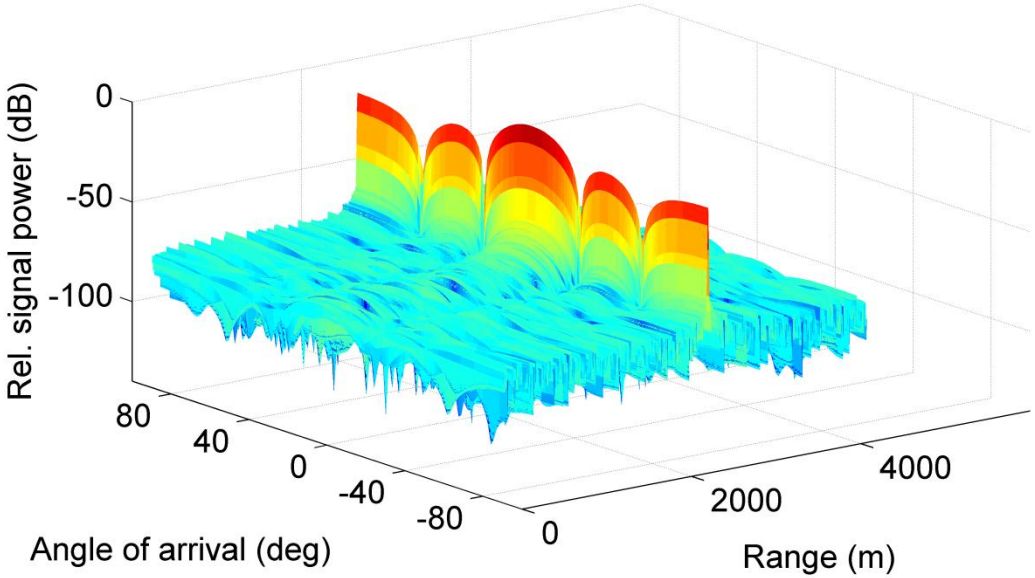
FPGA Output – Data Cube

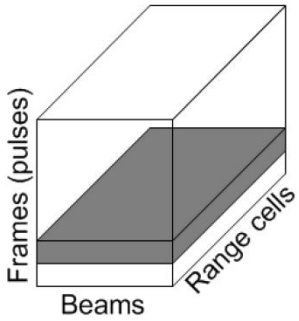
CW





LFM





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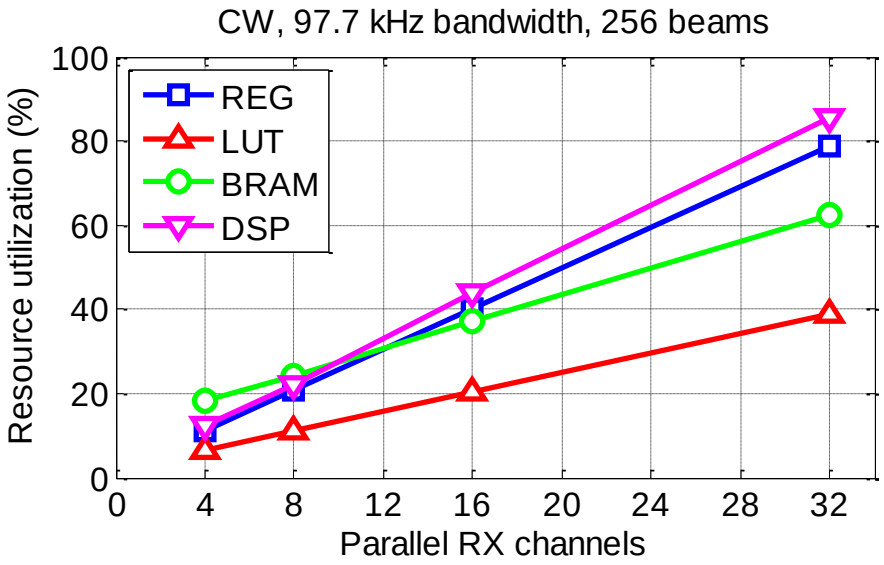
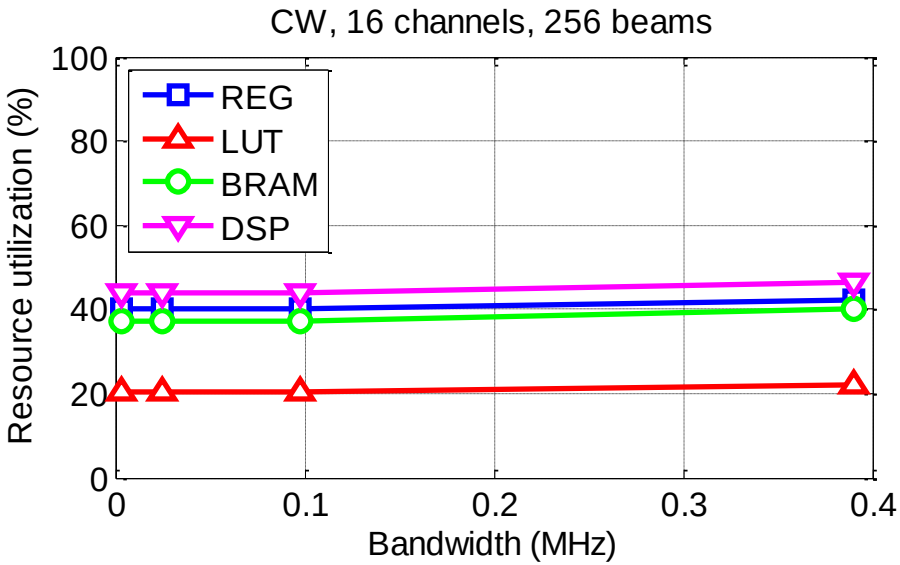
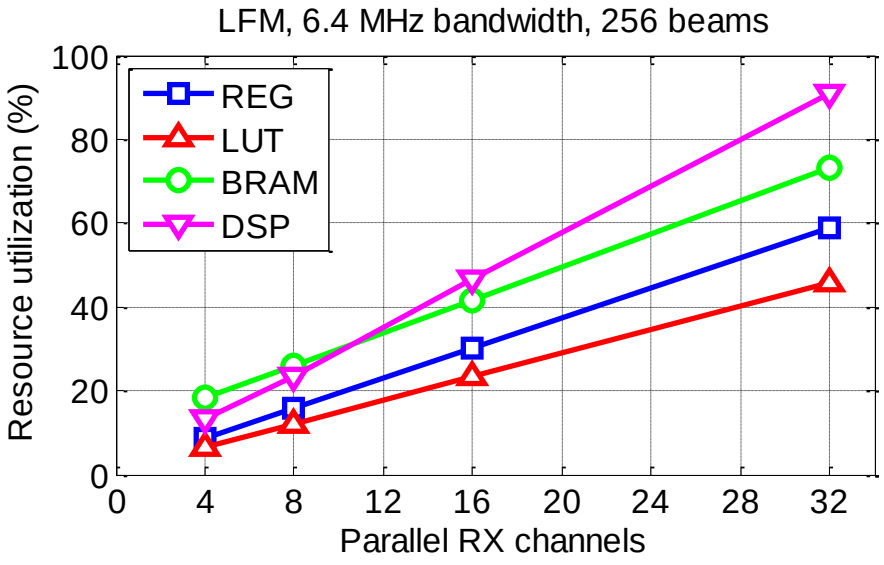
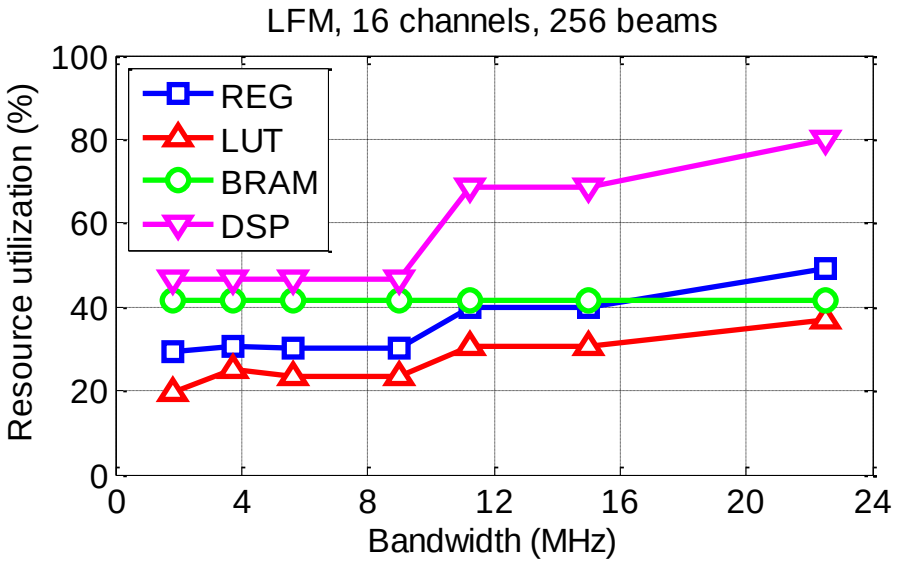
Scaling number of RX channels and bandwidth









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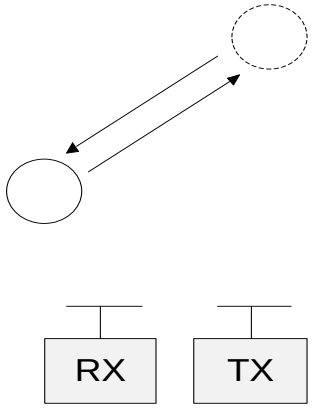
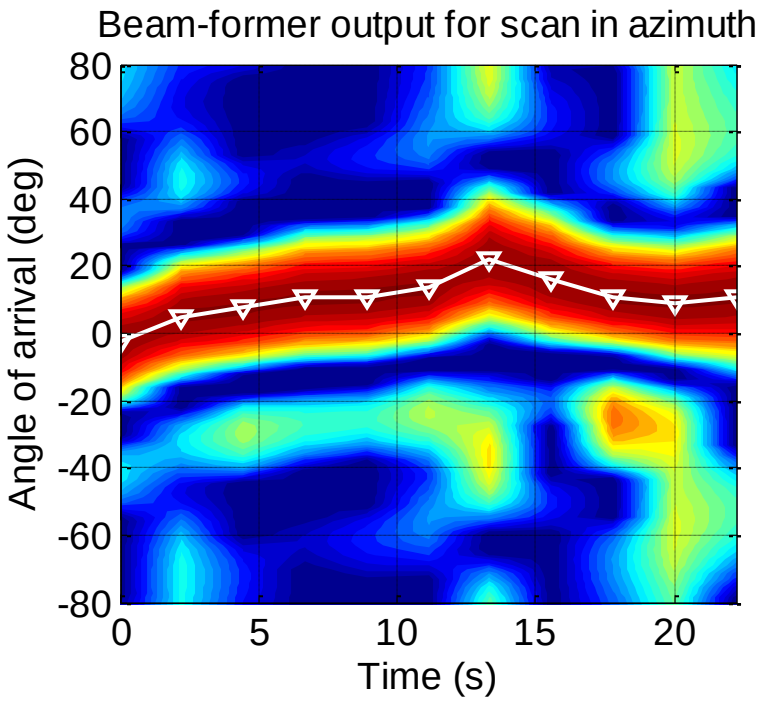
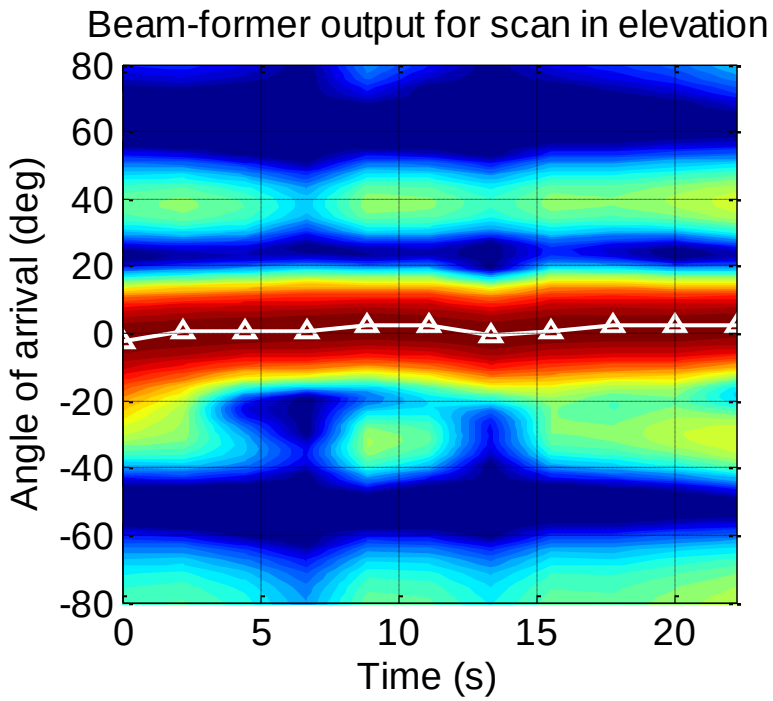
Radar Measurements

- Close mono-static setup
- CW radar end-to-end test
  - Direction finding
  - Doppler







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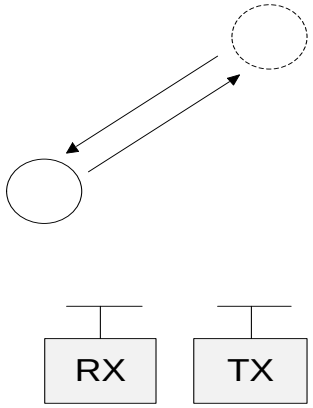

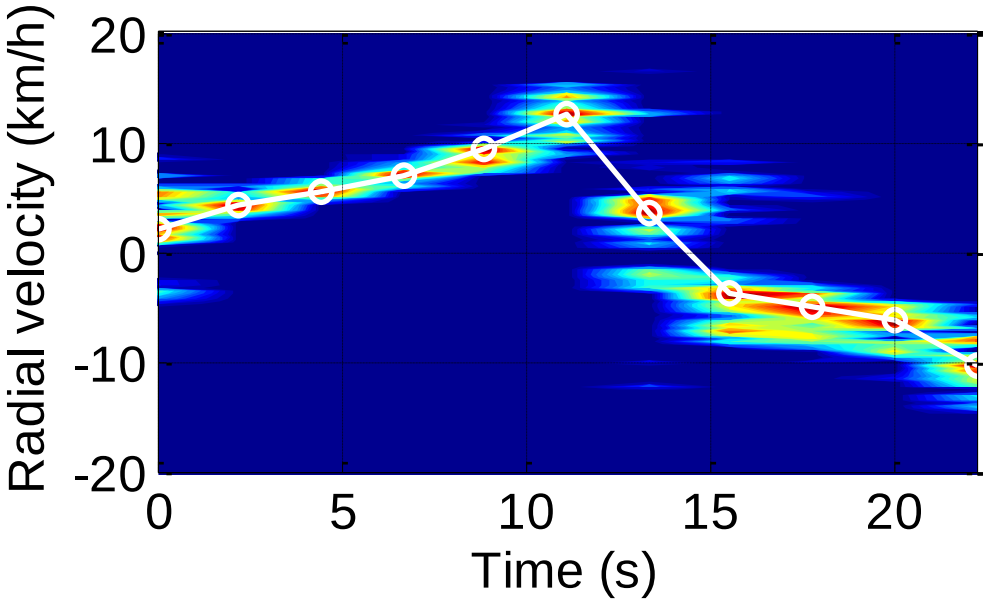

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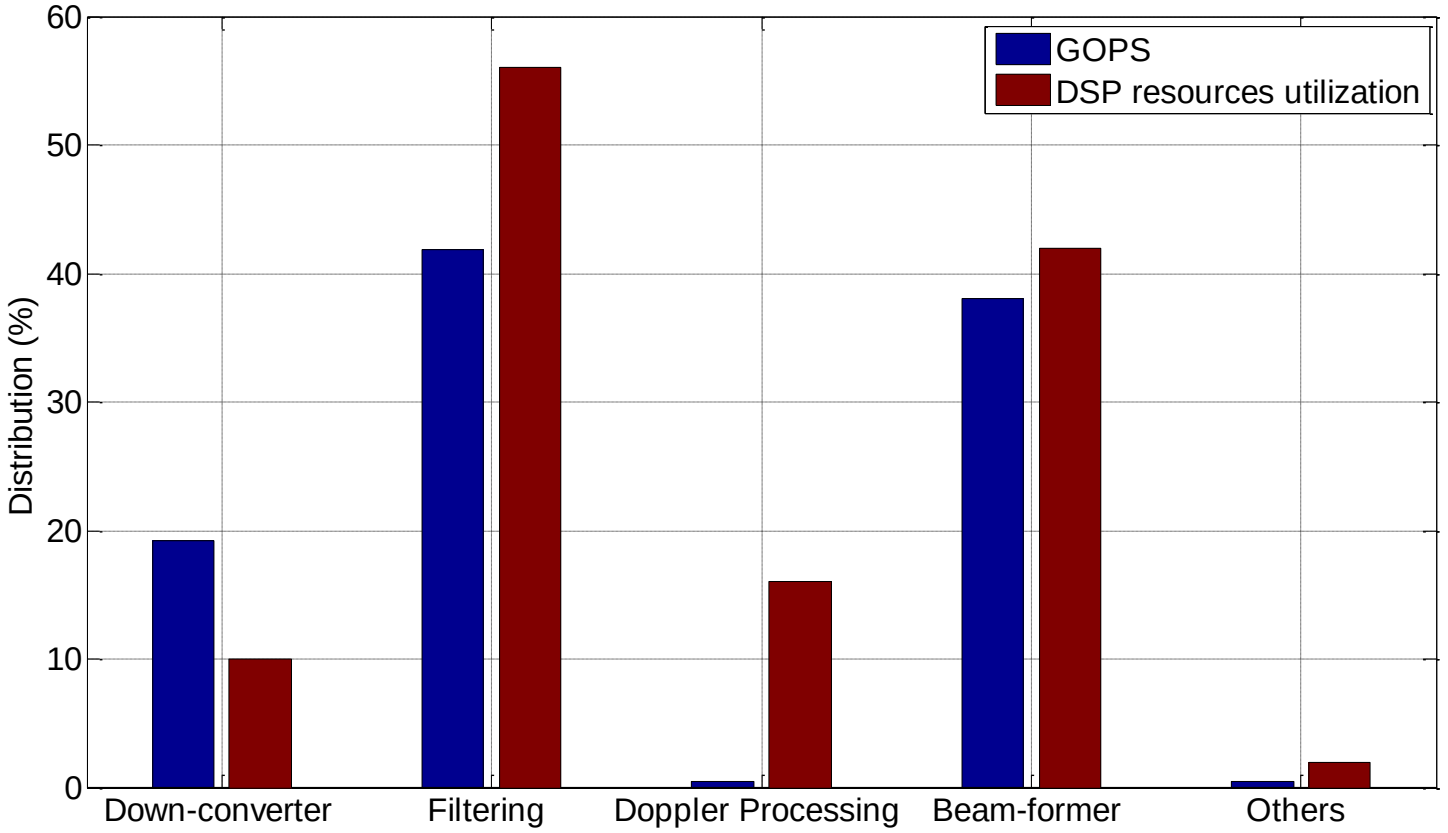
Summary and Outlook

- Mini-Radar to serve as an experimental reference system
- Full radar development from scratch
- Flexible FPGA signal processing implementation
  - Waveform flexibility
  - Scalable in number of channels, bandwidth, number of beams, and processing throughput
- Estimation of computational complexity of the receiver signal processor in terms of FPGA resource consumption
- System tests to validate the Mini-Radar system
- Future activities:
  - Further signal processing techniques (such as pulse-to-pulse-processing)


Thank you for your attention!

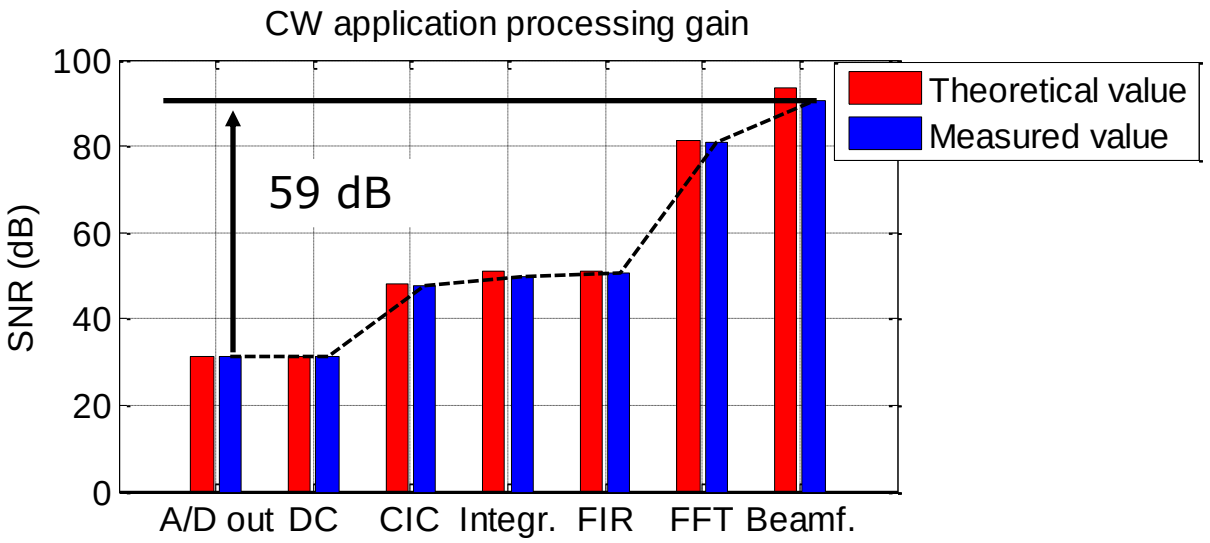
Annex

Comparison GOPS – DSP Slices

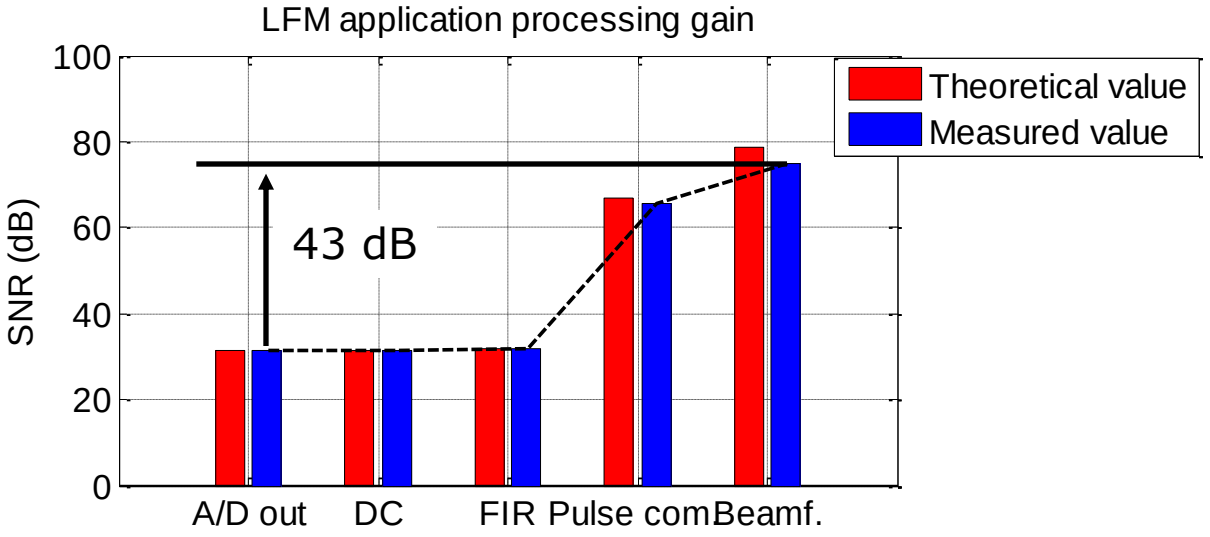


Processing Gain Measurements

CW



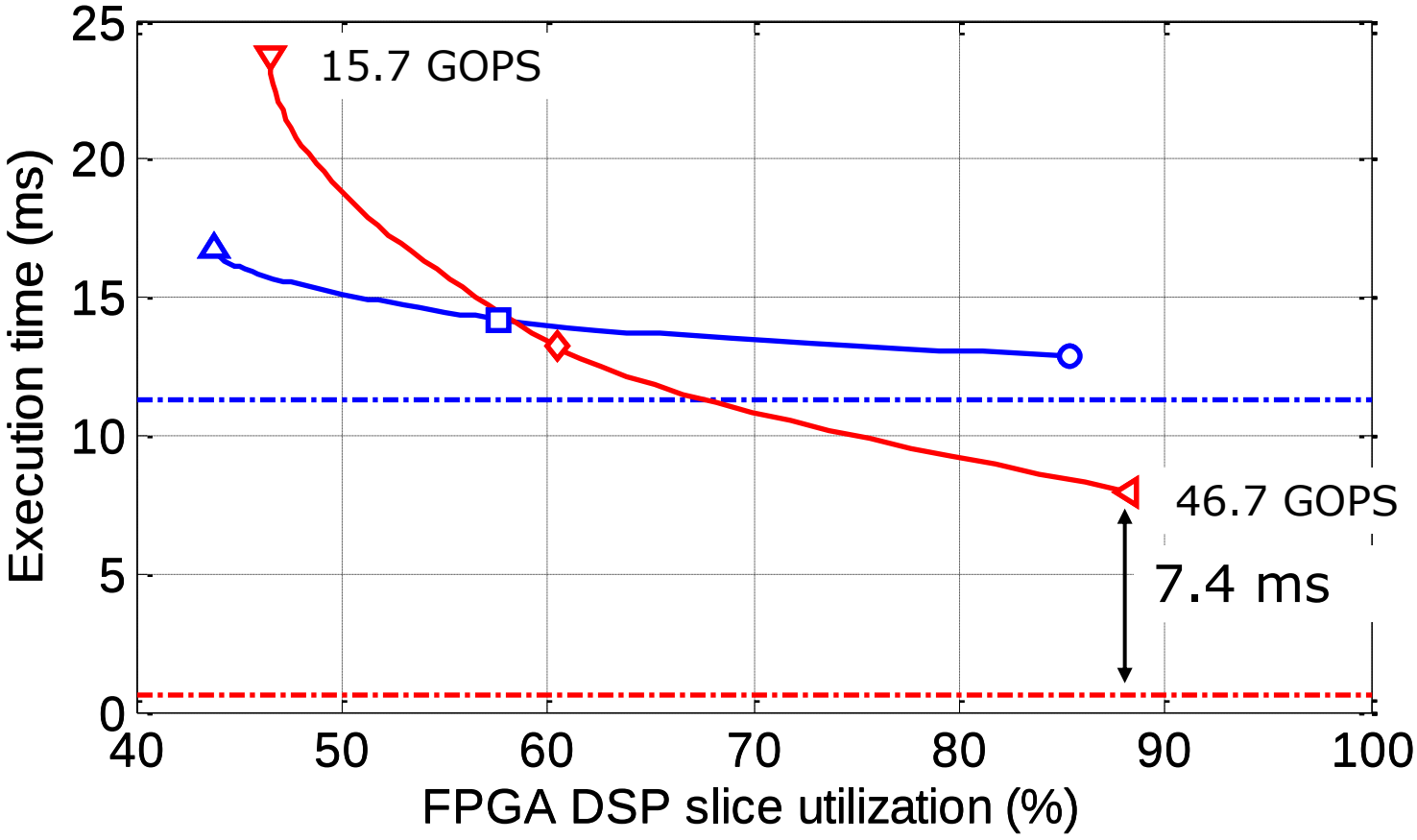
LFM



Mini-Radar link budget

System properties	Transmit power	40.0	dBm
	Required SNR	20.0	dB
Target properties	Target RCS (metallic sphere with 0.5m radius)	-1.1	dBm^2
Antenna properties	Transmit antenna gain (phased array antenna)	16.0	dBi
	Receive antenna gain (single element)	6.0	dBi
Receiver noise	Receiver noise temperature at 1st LNA input (290K physical temperature)	170.4	K
	Analog front-end noise bandwidth	8.8	MHz
System losses	Receiver cable and additional losses (due to implementation imperfections)	2.6	dB
CW Operation			
Receiver processing gain		59	dB
Required signal power at 1st LNA input		-145.7	dBm
Reference range		**9063**	**m**
LFM Operation			
Receiver processing gain		43	dB
Required signal power at 1st LNA input		-130.3	dBm
Reference range		**3742**	**m**

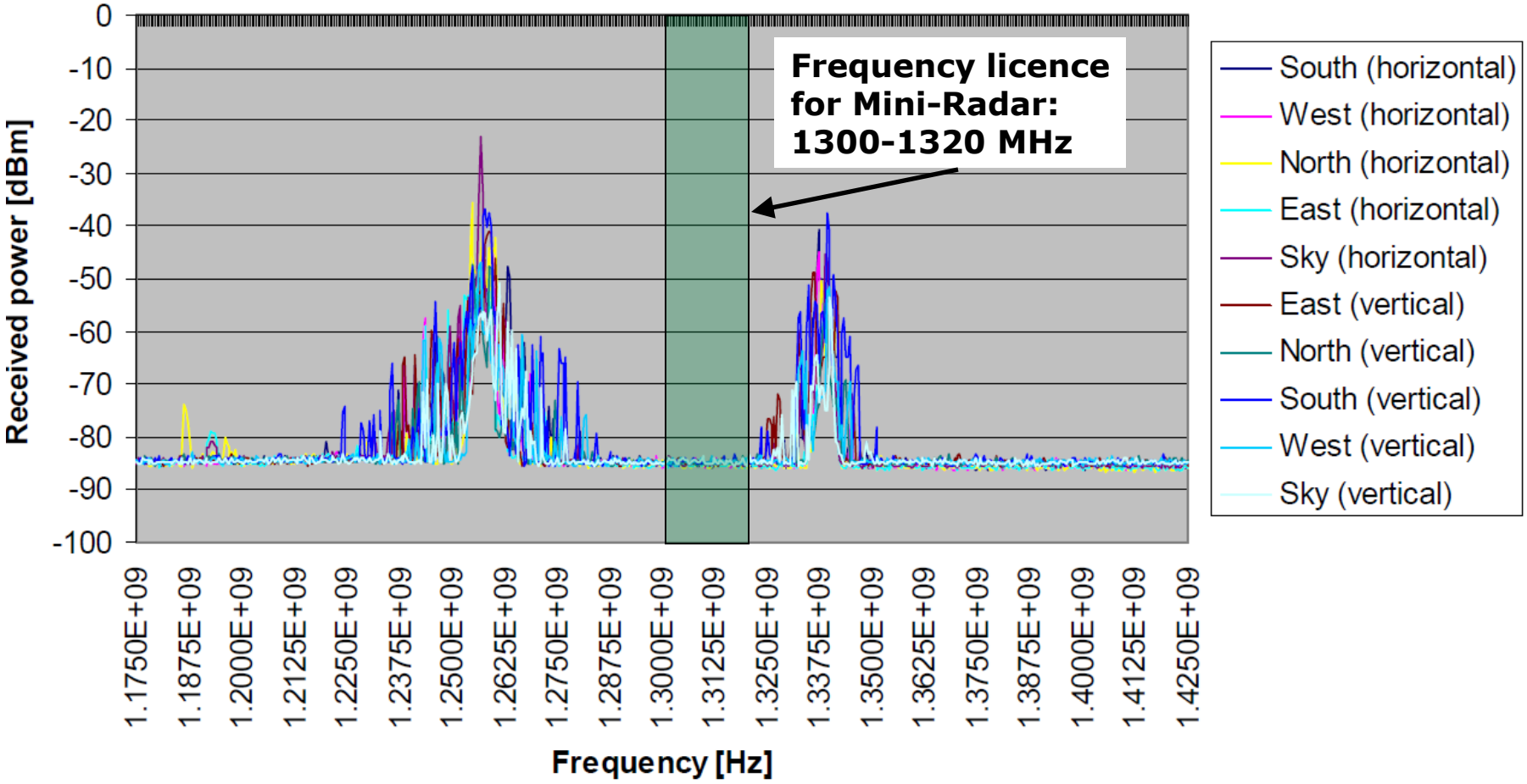
Scaling throughput



16 RX channels, 6.4 MHz bandwidth (LFM), 256 beams

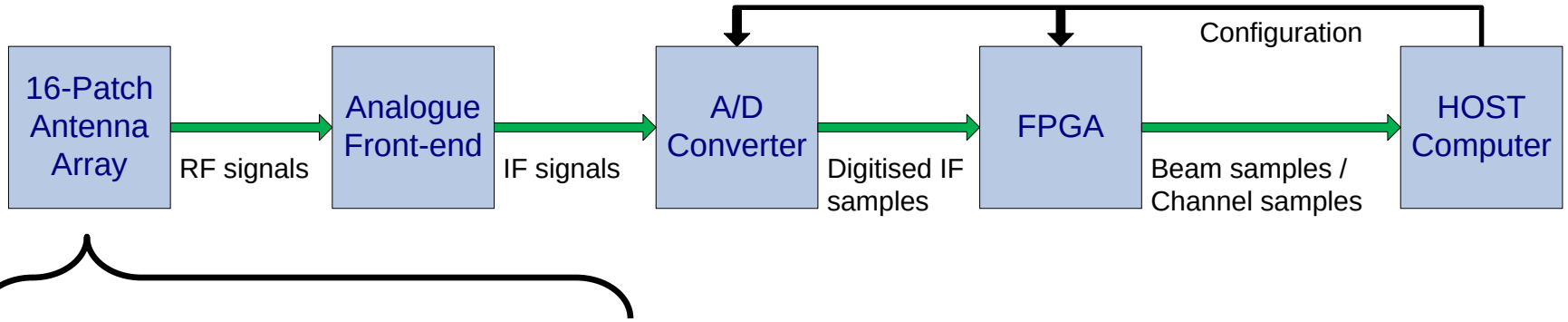
Frequency choice & licence for Mini-Radar

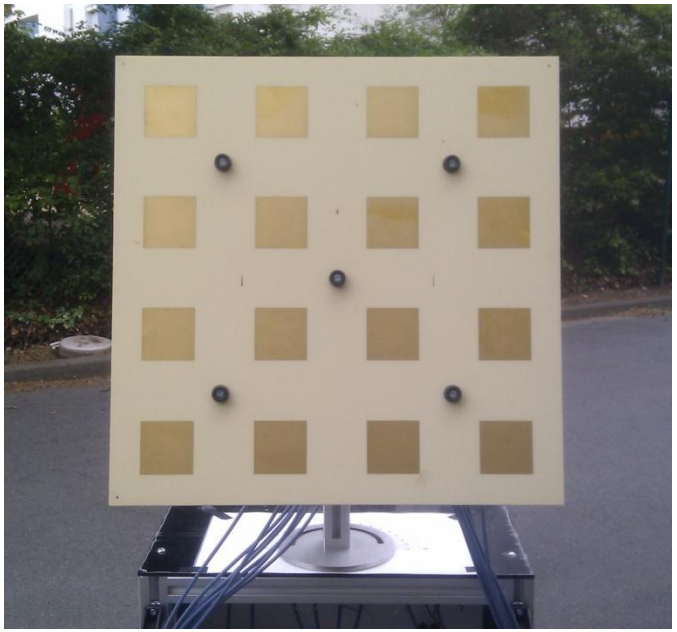
Measurement of interferers within radar band to find a good frequency for the Mini-Radar



Mini-Radar system design: Receiver

Receiver block diagram





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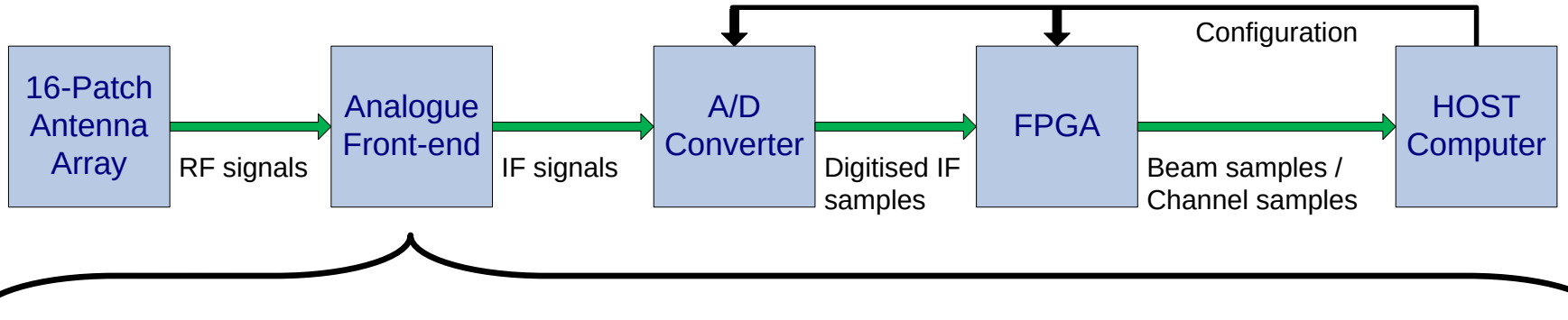

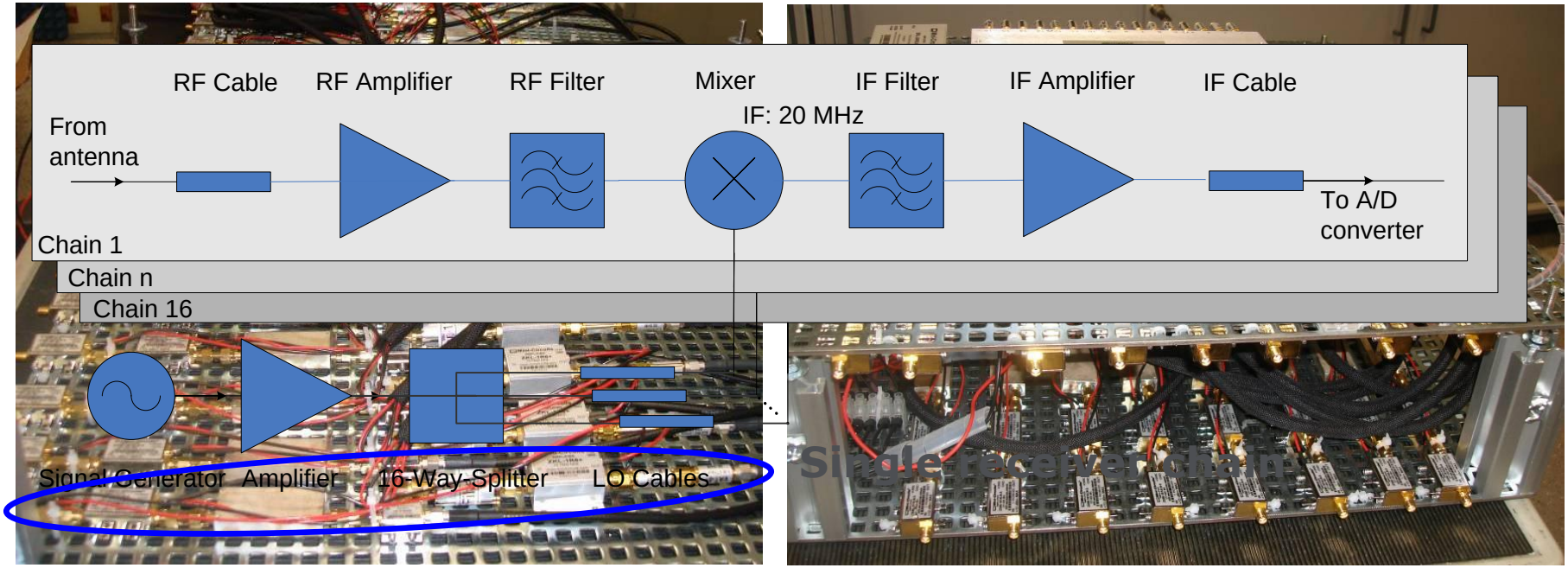

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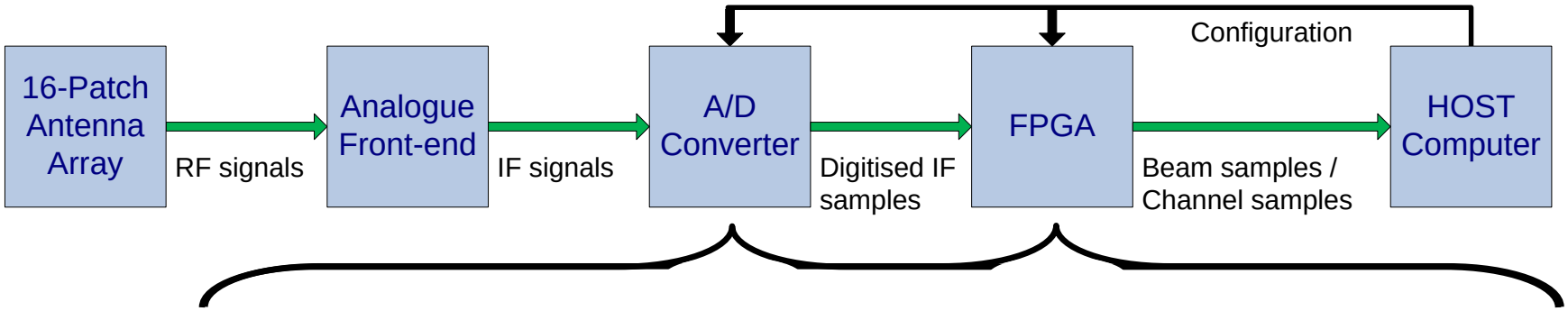

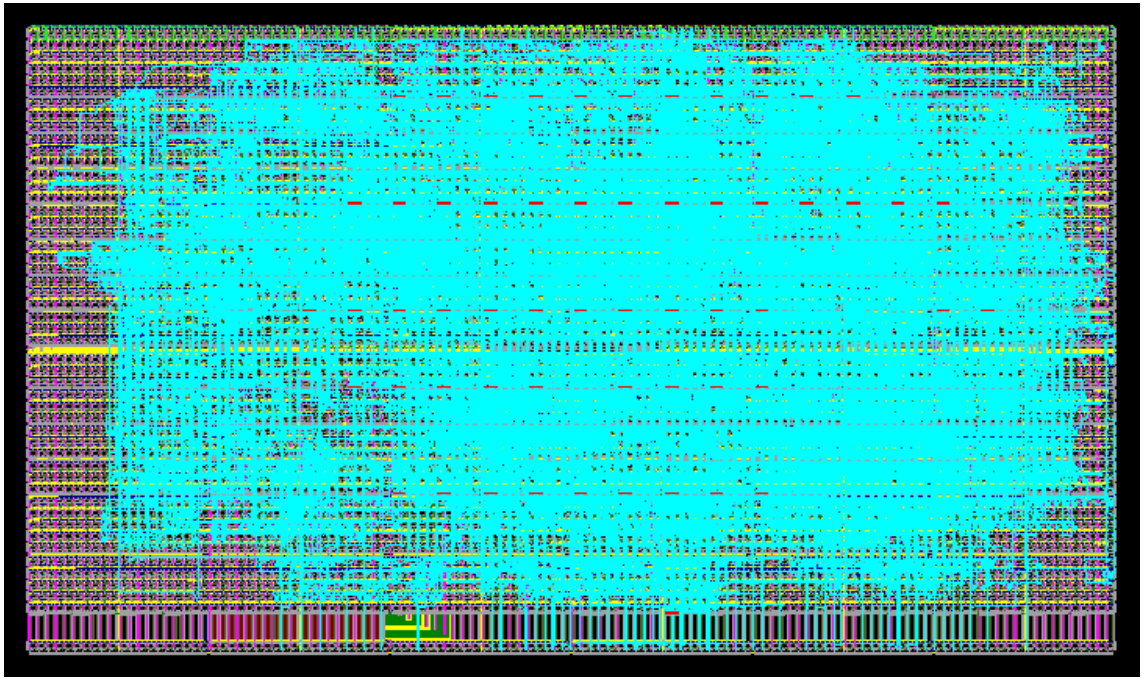

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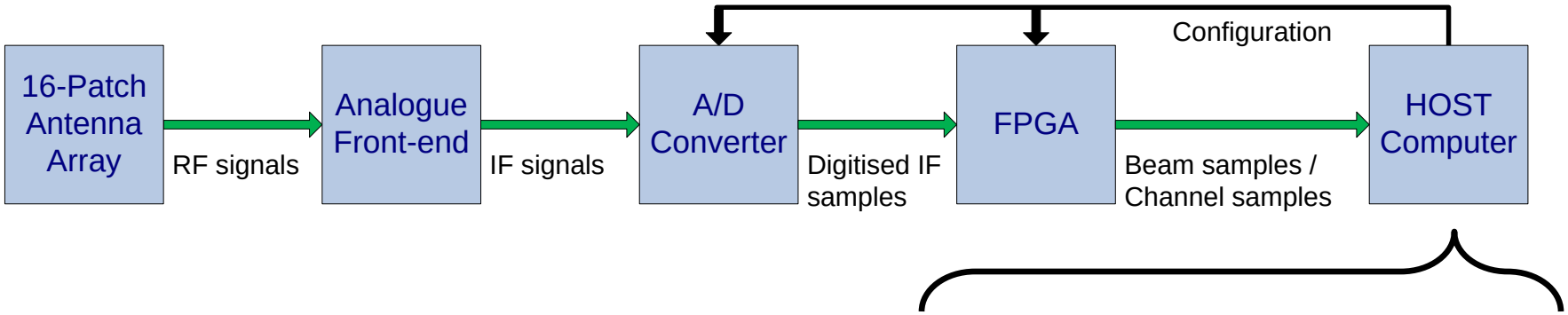
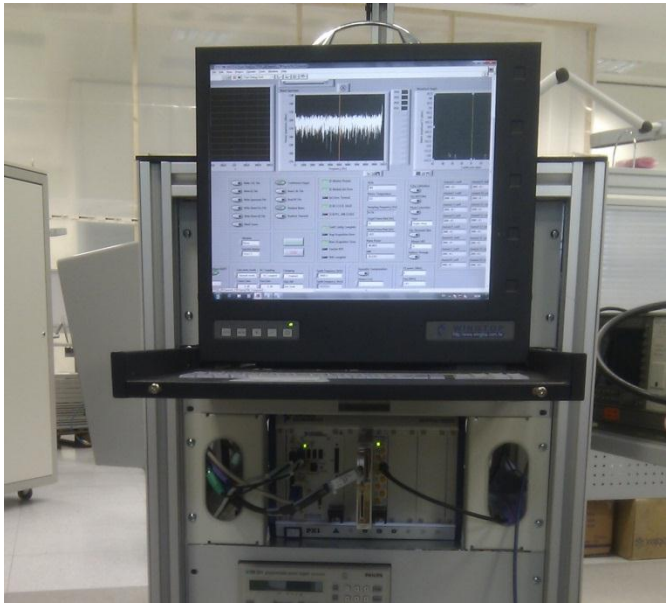
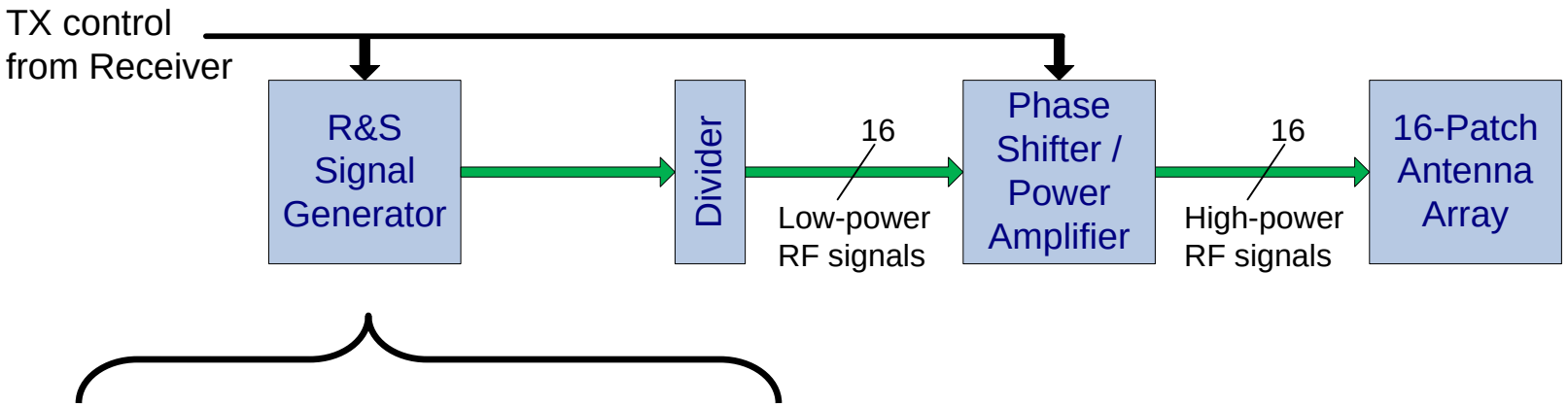




Mini-Radar system design: Transmitter

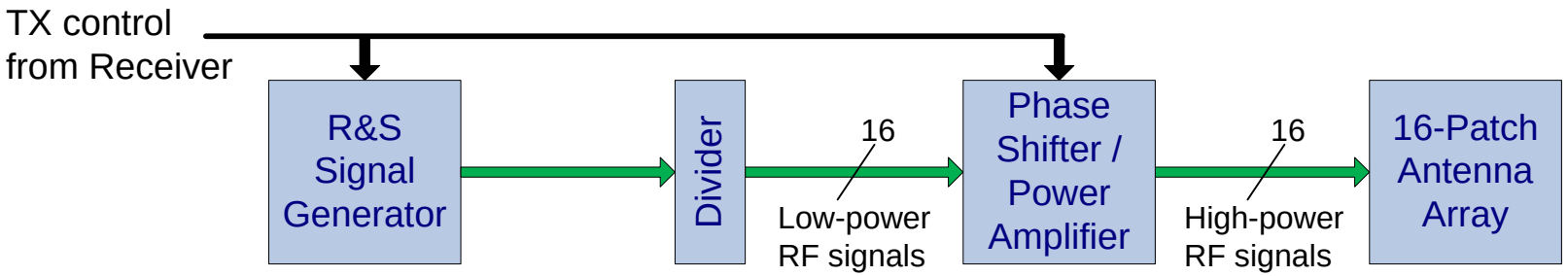
Transmitter design (signal generator)



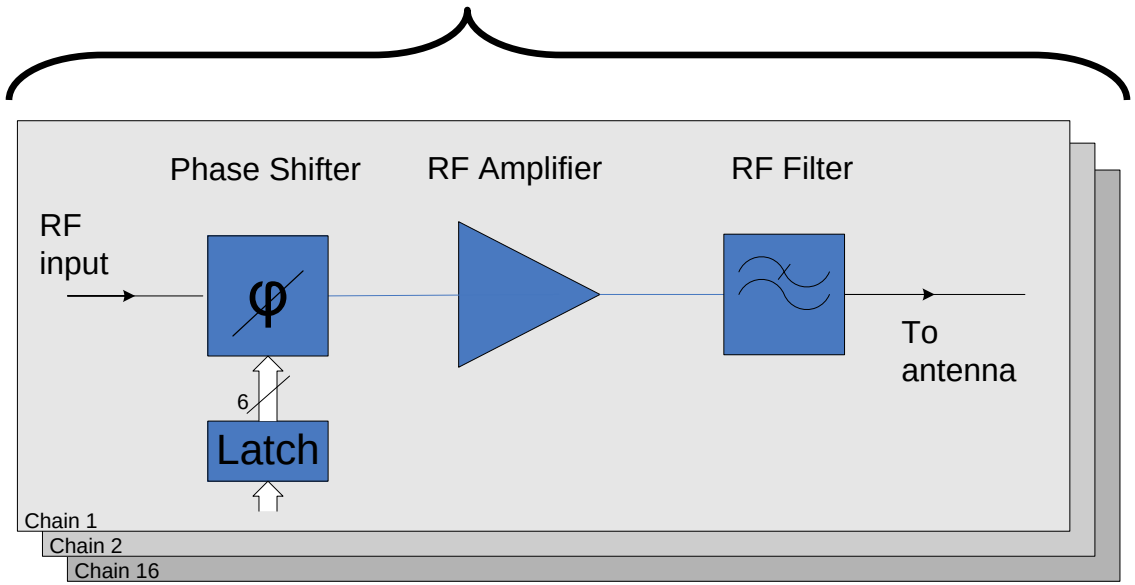
- Arbitrary waveform generator

Mini-Radar system design: Transmitter

Transmitter design (phase shifter / power amplifier)



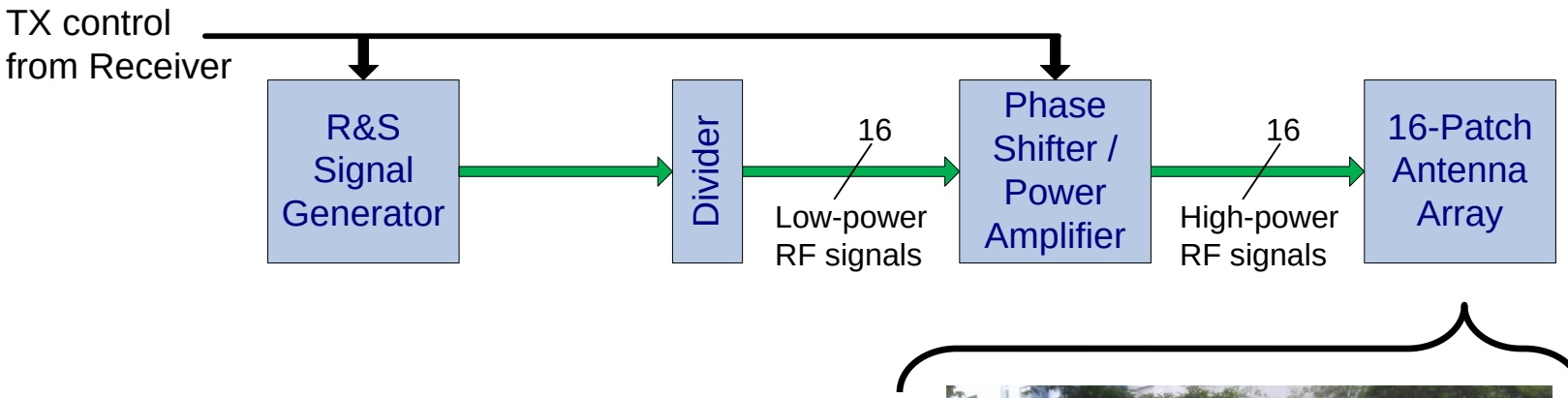
- 16 parallel modules
- Digitally-controlled phase shifter (360°, 6 bit)
- Power amplifier (1 Watt output, 30 dB gain)
- Output low-pass filter
- Design and manufacturing by external supplier



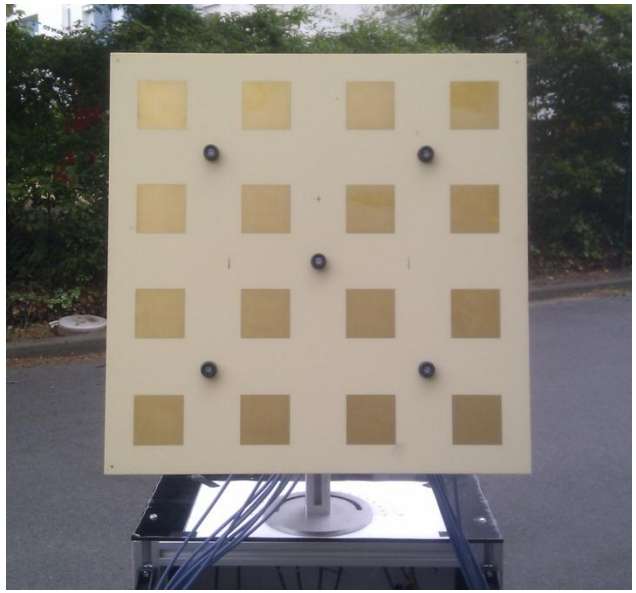
Becker Nachrichtentechnik GmbH

Mini-Radar system design: Transmitter

Transmitter design (antenna)



- 16 element patch antenna array
- Dual polarization (horizontal + vertical)
- Same design as receive antenna

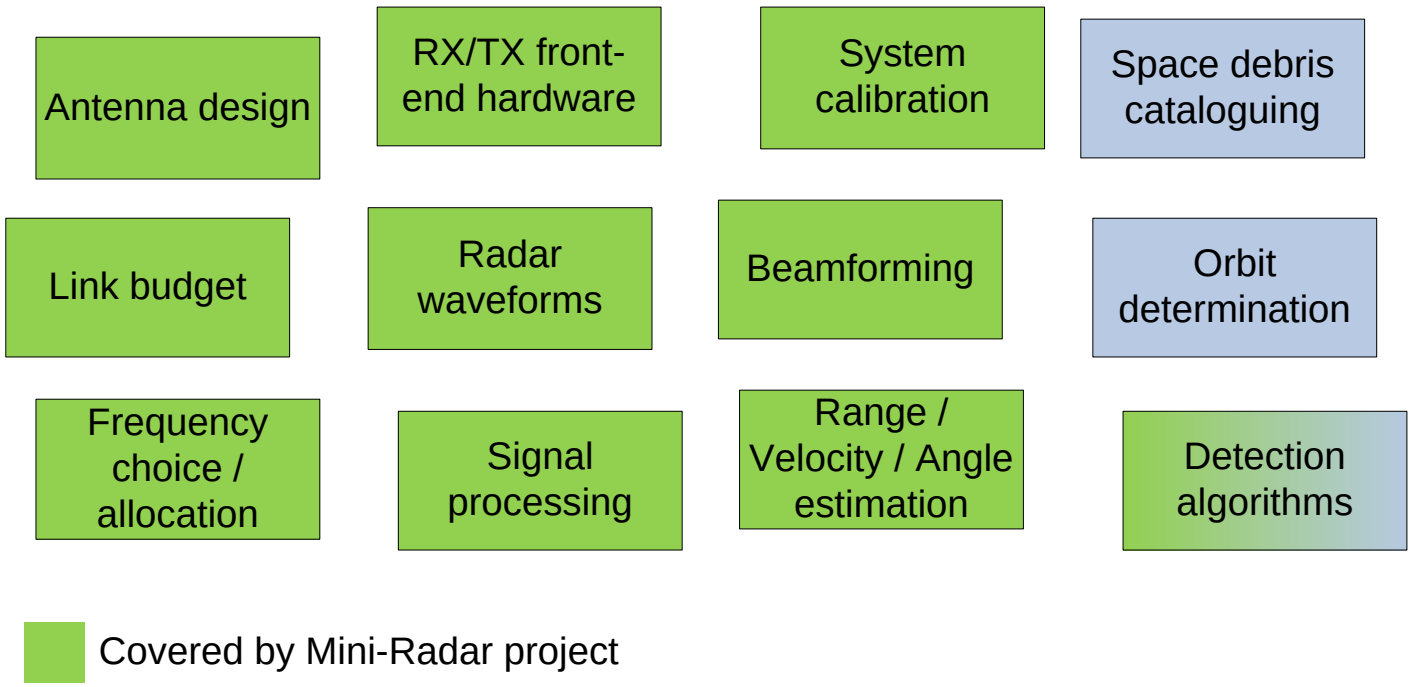


Mini-Radar project

Mini-Radar project

- Develop a small-scale radar demonstrator
- Support industrial SSA radar developments
- Build up internal experience

SSA radar system building blocks



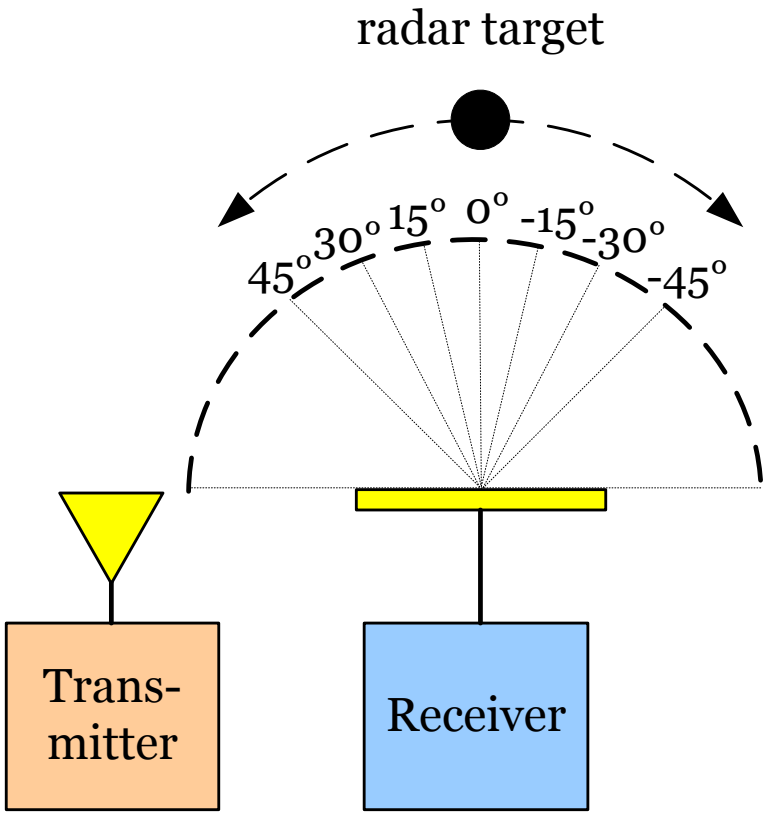
Mini-Radar direction finding

Measurement setup: Direction finding

Radar measurement setup:

- Phased array receiver
- Determine direction of reflected signal via beam-forming
- MTI filter for clutter suppression

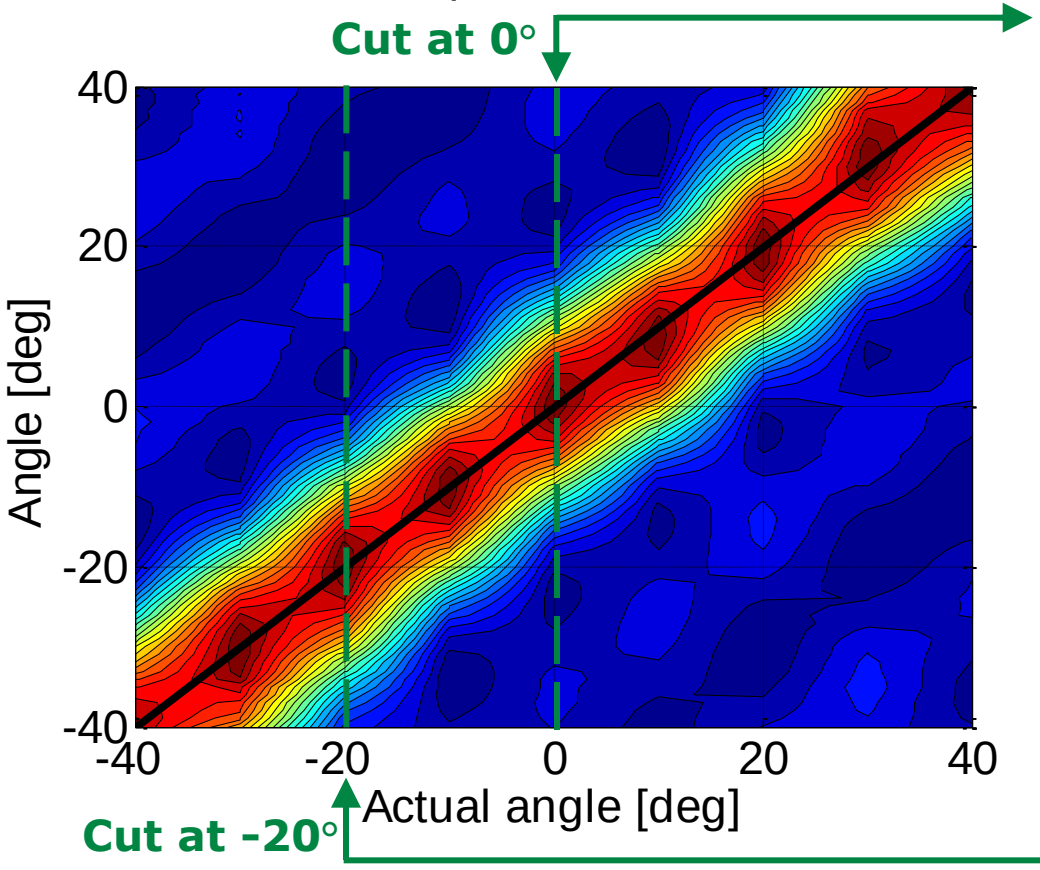
-> Validate receiver beam-forming

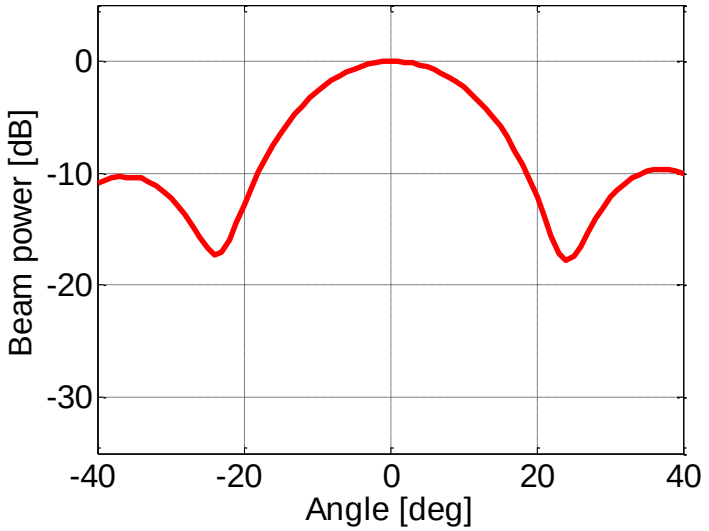


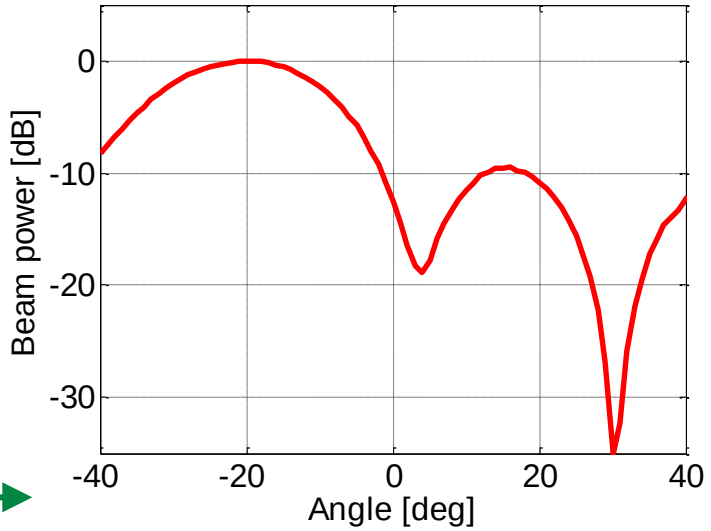
Mini-Radar
beam-forming measurements

Receiver beam-forming: Beam-forming angle versus angle of actual signal direction.

Red: high signal power
Blue: low signal power
Black line: expected maximum value







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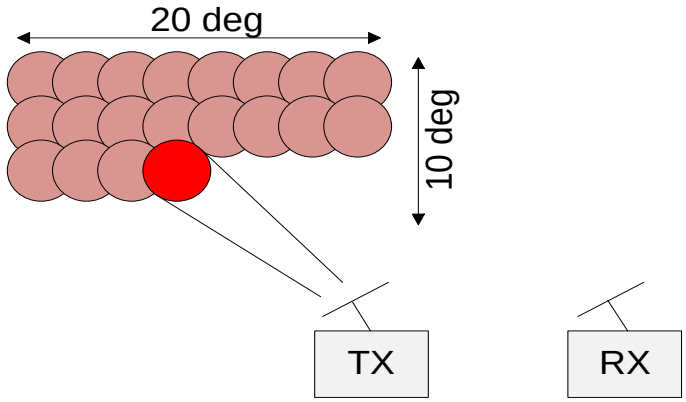

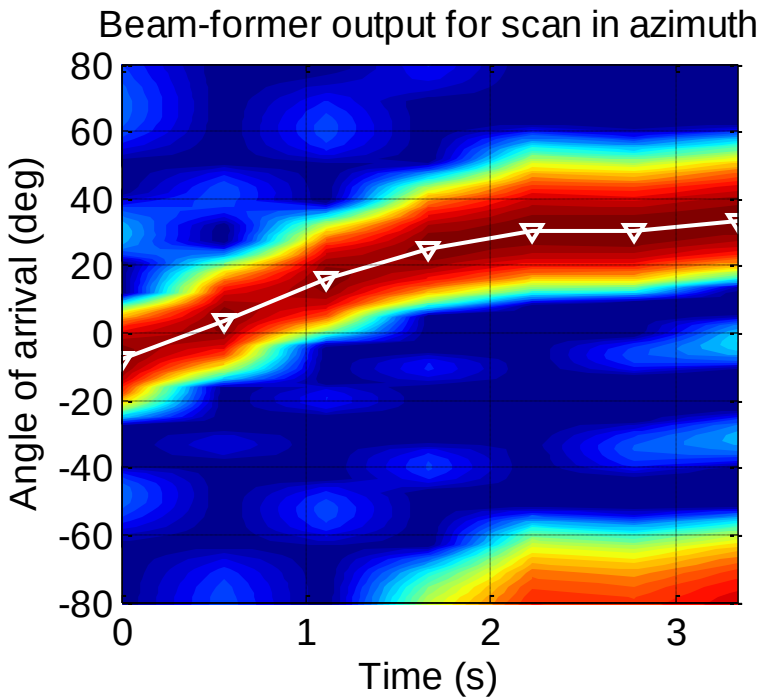

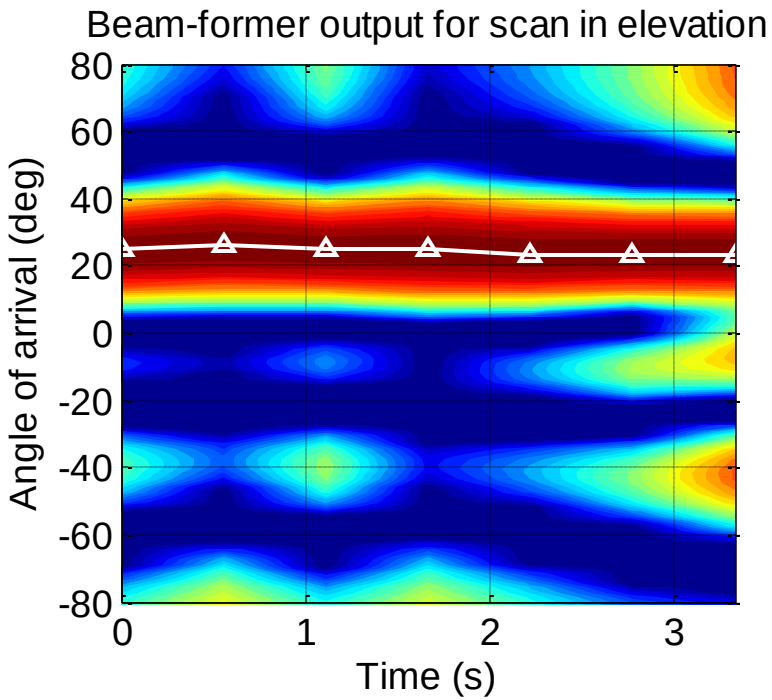

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