Analysis of Yield Loss due to Random Photolithographic Defects in the Interconnect Structure of FPGAs

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ABSTRACT

This paper presents an analysis of the potential yield loss in FPGA due to random defects in metal layers. A proven yield model is adapted to target the FPGA interconnect layers in order to predict the manufacturing yield. Defect parameters from the 2003 SIA roadmap are used to investigate the trend in yield loss due to defects in interconnect layers in the future. It is shown that the low yield predicted for the 45nm technology node and beyond is a cause for concern. The potential impact on yield using two different approaches, namely redundant circuits and fault tolerant design, is also presented.

Categories and Subject Descriptors

B.8.1 [**Hardware**]: Performance and Reliability—*Reliability, Testing, and Fault-Tolerance*; B.7.3 [**Hardware**]: Integrated Circuits—*Reliability and Testing*

General Terms

Reliability

Keywords

yield prediction, FPGA interconnect, FPGA redundancy, fault tolerance, yield enhancement, interconnect model, interconnect faults, catastrophic faults.

1. INTRODUCTION

The area occupied by wiring channels and interconnect configuration circuits in an FPGA is significant, occupying 50 to 90 percent of the chip area [1]. With current trends aiming to reduce the area occupied by wiring segments in the routing channels, wire width and wire spacing have been reduced. This has in turn led to higher occurrences of wiring defects, such as breaks and shorts, and decrease in manufacturing yield and fewer functioning devices at fixed manufacturing costs.

The most important contributors to manufacturing yield loss are failures caused by local unintended product-process interactions [2]. Device defects can be divided into three different categories [3]: 1) Gross defects, which will almost certainly cause a yield loss; 2) Parametric defects, which rarely cause yield loss, although could affect device performance and reliability; 3) Random defects, which are defined as any deviation from the original design, and will only affect yield under specific circumstances. Random defects can be further divided into two types: pinhole and spot defects. Pinhole defects occur in dielectric insulators; they are usually small and only account for a very small yield loss [4]. Spot defects are due to extra or missing material. Extra material often causes a short between two conducting paths, whereas missing material can cause an open. Since spot defects account for most of the yield loss in metal layers, it is this aspect that this paper examines.

The original contributions of this paper are: 1) to quantify the extent of the yield loss due to interconnect spot defects. The work is based on critical area analysis and yield prediction. We suggest an interconnect model, that represents the photolithographic patterns present in metal layers of a FPGA die. From this model, the portion of the area susceptible to defects is extracted and used in order to formulate a yield prediction model. 2) To estimate the yield of large FPGA devices in the future using defect parameters from the SIA roadmap predictions [5]. 3) To demonstrate the potential improvement in the overall yield by introducing two different defect tolerant approaches. By introducing redundant circuits to replace defective resources, or by adopting a fault tolerant design approach, it is possible to tolerate a small number of manufacturing faults and thus improve the overall manufacturing yield. 4) To explore the area overhead incurred by such fault tolerant schemes.

This paper is organised as follows: Section 2 gives a brief account of existing work in this field. Section 3 provides background information regarding critical area modeling and yield predictions. Section 4 introduces the metal layer model and the underlying assumptions of this study, while Section 5 provides the details of the SIA roadmap for the future. Section 6 offers an analysis of the results obtained and finally, Section 7 concludes the paper.

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2. PREVIOUS WORK

The problem of yield loss has been studied since the integrated circuit manufacturing process [6] began. As the electronics market expanded and more money was invested, the need to study economically viable solutions became apparent. Studies continued on the automation side, in order to make the manufacturing process as precise as possible [7]. Designers discovered that semiconductor device yield is determined primarily by the defect density and the critical area, i.e. the portion of the circuit active area in which the occurrence of a defect results in yield loss [8].

Research concentrated on these two aspects, and on how to improve the manufacturing process. Mathematical models were introduced to calculate the critical area of a given device and to predict yield [3, 4, 8]. All of this work is based on some underlying assumptions, many of which are still the subject of investigation [12].

With the ever increasing yield loss due to manufacturing defects, research was conducted to offer suitable solutions to limit the losses. One of the solutions came in the form of hardware redundancy. Hardware redundancy was easily implemented in memory chips, with great yield advantages at very low extra costs [13]. The regular structure of memory chips facilitates the implementation of extra circuitry that can be swapped in or out. Such improvement in yield is, however, not found in non-memory type of circuits. It proved too difficult to replicate enough hardware to significantly improve the yield of large VLSI circuits. This lead designers to adapt their designs in order to offer the least chance of defects. Techniques such as critical area reduction and via replication were used [16]. More recently, pre-layout techniques and manufacturing constraints were introduced [14, 15].

With regards to the programmable logic industry, and FPGAs in particular, much work has been carried out from a manufacturing yield point of view. The studies proposed were based on the assumption that the highly regular structure of most FPGAs is ideal to implement hardware redundancy. In particular, the authors in [26] proposed the first hardware redundancy technique. Introducing hardware redundancy however has a significant effect on the routability of designs; a study based on programmable interconnect faults is found in [25]. Howard *et al.* identified in their work [17] that the key to obtain a significant increase in the yield of FPGAs lies in fast reconfiguration. Their suggestion is to reconfigure a given design so that the faulty part of the chip is not used. This, in turn, would allow the use of partially defective devices, at the cost of extra computation needed to overcome the defect.

Most of the works has exclusively targeted the logic cell array [18, 19, 20, 21, 22, 23, 24]. An in-depth analysis of the techniques proposed to increase FPGA yield is given in [18]. This study presents fault tolerant techniques to increase the yield of FPGAs by reconfiguring factory detected faults in the logic cells and interconnect. It backs up its statements with a yield analysis based on logic cell array defects.

To the best of our knowledge, none of the existing work explores the effect of spot defects on the yield of FPGA devices due to interconnect faults. This paper further explores the consequences of introducing fault tolerant schemes on the manufacturing yield in large FPGA devices.

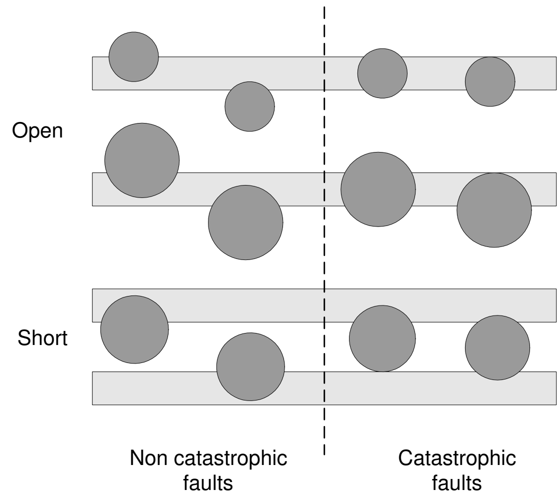

Figure 1: Catastrophic faults relative to size. Similar sized defects may only cause a fault if a pattern is broken or two patterns joined

3. BACKGROUND

This section explains the concept of critical area and how it is used to predict device yield. Defects are assumed to be circular in shape, with a diameter x. The critical area analysis applies to metal patterns drawn on a single fabricated metallization layer. Modern chips are constructed with multiple metallization layers, meaning that the critical area analysis has to be carried out for each layer, with different parameters. Unless specified, the yield only refers to a single metal layer yield.

3.1 Critical area

The critical area of a lithographic pattern is defined as the portion of the total chip area within which the occurrence of a defect results in a fault [8]. In more general terms, a defect of size x will only cause a fault if its center falls in a particular section of the chip, as shown in Figure 1. Figure 1 shows how defects of equal size may or may not cause a catastrophic fault, depending on where their center falls.

The critical area is defined in (1):

$$A_C = A_{Total} \int_0^\infty K(x)S(x)dx \quad (1)$$

where A_{Total} is the total die area, x is the defect size, $K(x)$ is the fault probability kernel, and $S(x)$ is the defect size distribution. The integral term is sometimes referred to as $\phi(x)$, the *fault probability.* Figure 2 shows a graphical representation of these functions.

The fault probability kernel shows how the portion of the defect-sensitive chip area varies as the defect size varies. For the purpose of simplicity, only the case for a single metal line susceptible to an open fault is shown.

The critical area for open defects for a single, metal interconnect is depicted in Figure 3 as the area sandwiched by the two dotted lines. The total area is thus $L(w + 2h)$, and $h = x/2 - (w - d)$. w is the width of the conducting paths, and d is defined as the minimum strip of metal needed in order to guarantee conduction. In our model, it was assumed

that *d=0*. The fault probability kernel $K(x)$ is shown in Figure 2.

There has been much discussion regarding the defect size distribution [9]. It is now widely accepted that $S(x)$ should be zero until the defect size reaches the minimum feature size x_0 (see Figure 2), and falls away from a maximum value as a function that is inversely proportional to the cube of the defect size [3]. Defects of size smaller than x_0, mainly due to process related dirt, are not considered as they will not result in a catastrophic fault.

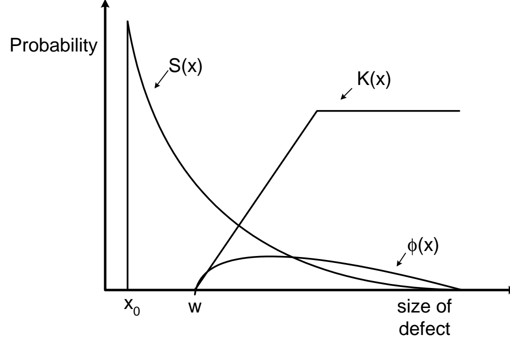

Figure 2: Fault probability kernel $K(x)$, defect size distribution $S(x)$, and fault probability $\phi(x)$. Note that the majority of defects have size similar to the minimum feature size x_0

3.2 Yield equations

For a non-constant defect density, the probability of finding n defects in a chip of critical area $A = A_C$, assuming a defect density D, is given by (2), where $f(D)$, α and B are defined by (3). α is known as the *clustering parameter*, whereas D_0 is known as the *average defect density*[3].

$$p(n, A, D) = \int f(D) \frac{(AD)^n e^{-AD}}{n!} dD \quad (2)$$

$$f(D) = \frac{1}{\Gamma(\alpha) B^\alpha} D^{\alpha-1} e^{\frac{-D}{B}},$$

$$\alpha = \frac{D_0^2}{var(D)}, B = \frac{var(D)}{D_0} \quad (3)$$

Combining (2) and (3) results in (4)

$$p(n, A, D) = \frac{\Gamma(\alpha + n)}{n!\Gamma(\alpha)} \frac{(AD_0/\alpha)^n}{(1 + AD_0/\alpha)^{n+\alpha}} \quad (4)$$

As the yield is the probability of obtaining defect-free chips, the yield prediction is made using (5)

$$Y = p(0, A, D) = \frac{1}{(1 + AD_0/\alpha)^\alpha} \quad (5)$$

For a chip with redundancy, called an n-redundant chip, where n is the maximum number of tolerable faults, the total yield will be made up of chips exhibiting 0,1,2,3...,n faults. The total yield for an n-redundant chip is:

$$Y_{n-redundant} = p(0, A, D) + p(1, A, D) + ... + p(n, A, D) \quad (6)$$

If we assume that the majority of chips will have either 0 or 1 fault, the resulting equation for the yield of chips exhibiting a maximum of one fatal fault is thus given by (7)

$$p(1, A, D) = \frac{AD_0}{(1 + AD_0/\alpha)^{\alpha+1}} \quad (7)$$

And the yield of a chip able to function in the presence of one fault is given by (8)

$$Y_{1-redundant} = \frac{1}{(1 + AD_0/\alpha)^\alpha} \frac{\alpha AD_0}{\alpha + AD_0} \quad (8)$$

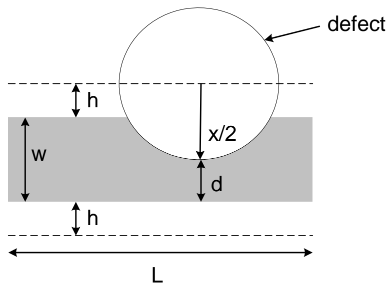

Figure 3: Parameters in the fault probability kernel $K(x)$. L, w and d are architectural parameters, while h is dependent on x, the size of the defect

3.3 Multiple layer yield model

Modern dies are made up of multiple metallization layers. The critical area analysis, however, only refers to a single plane, with specific lithographic patterns on it. If the yield of layer i in an m-layer die is denoted by Y_i, then the die yield is given by (9), from [10]:

$$Y_{die} = \prod_{i=1}^{m} Y_i \quad (9)$$

From (9), it is easy to understand how a small yield loss in one layer could degrade the overall yield of the die. For example, in a 10 interconnect layer die, a yield loss of 5% per layer over all layers will result in a total die loss of 40%.

4. INTERCONNECT YIELD MODEL

FPGAs have, by nature, a regular, repeating structure. Their logic architecture is formed by an array of identical logic blocks and switch matrices. As a result, all the metal connections between logic blocks are also regularly shaped and distanced.

FPGAs offer lines of specific length to connect one logic block to another. An interconnect metal layer can therefore be modelled as a collection of lines of similar length, grouped in channels, leading from one logic block to another. A model of a possible metal layer design is shown in Figure 4.

The parameters used to define the model are defined below:

- M - width and height of CLB array in the FPGA. The device is assumed to be a square array of MxM CLBs.
- *lines* - Number of interconnects in a wiring channel.
- L - Length of line. This measure differs depending on the metal layer (see Figure 3).
- w - width of the conduction path.
- s - space between conducting paths.

For simplicity purposes, it is assumed that the width and the space between paths have identical size. The size of each parameter can then be found by halving the wire pitch value. Short lines are manufactured at the lower layers, whereas the higher layers will host the longer, global lines.

All inter-layer patterns (vias, contacts) are assumed to be contained in the areas above the switch matrices. It is therefore possible to model all lines as straight, parallel patterns equally spaced between each other. The patterns are only broken over the switch matrices, which are regularly arranged in the FPGA logic array.

The predicted array size is calculated assuming that M is approximately inversely proportional to the minimum feature size. It is further assumed that halving the minimum feature size will result in doubling the parameter M.

With regards to the metal layers, it is assumed that the silicon space is used to a maximum, i.e. there are no free areas on the silicon. Area not occupied by the metal lines maybe be occupied by vias and contacts, but no free area is left on the silicon.

The defects, for simplicity purposes, are assumed to have circular shape, with diameter x.

Calculating the fault probability kernel for such a structure is a relatively trivial task. For open defects, the fault probability kernel is shown in (10)

5. SIA PREDICTIONS

This section provides a brief summary of the relevant predictions made by SIA as regards to interconnect dimensions [11]. Table 1 provides a list of the dimensions relevant to this paper.

Note that for some of these solutions, manufacturable solutions are not known. This in particular applies to the 22nm technology node. For the most of the other predictions, solutions are known and already being tested in large volumes. For those parameters which do not have a manufacturable solution, the SIA roadmap offers an indication of the dimensions likely to be obtained.

Figure 5 shows a typical cross section of a modern device [11].

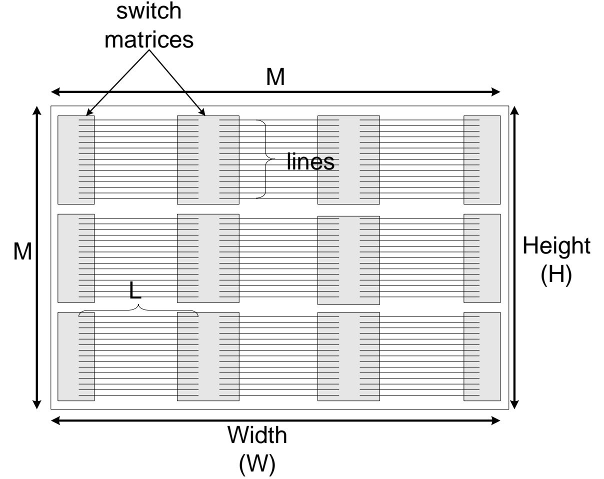

Figure 4: Interconnect metal layer. The gaps between the metal lines account for vias connections between layers

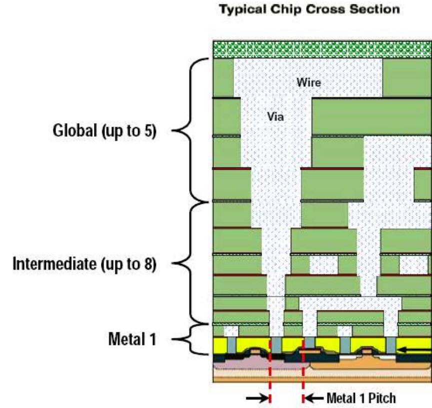

Figure 5: Typical device cross section [11]

6. RESULTS

Using the proposed model and the information provided by the SIA roadmap, it is possible to analyze the predicted yield of interconnect layers with different characteristics. This allows the prediction of current and future yields, and the exploration of potential benefits of different fault tolerant schemes.

$$K(x) = \frac{1}{A_{Total}} \begin{cases} 0 & x < w \\ M * lines * (L + \sqrt{x^2 - w^2}) * (x - w) & w \le x < s + 2w \\ H * M * (L + \sqrt{x^2 - w^2}) & s + 2w \le x < \frac{W}{M} - L \\ H * W & x \ge \frac{W}{M} - L \end{cases} \quad (10)$$

Table 1: SIA roadmap for interconnects [11]

Year	2001	2004	2010	2016
Technology Node	hp130	hp90	hp45	hp22
Number of Metal Levels	9	10	12	14
Metal 1 wiring pitch (nm)	284	214	108	54
Intermediate wiring pitch (nm)	368	275	135	65
Minimum Global wiring pitch (nm)	580	410	205	100
Cluster parameter	2	2	2	2
Critical defect size (nm)	65	45	23	11
Overall electrical defect density D_0 $(faults/m^2)$	2210	2210	2210	2210
Random D_0 $(faults/m^2)$	1395	1395	1395	1395
Predicted array size (M)	120	160	300	550

In obtaining these results, the following assumptions are made:

- The biggest device is 1.5in X 1.5in for all technology nodes.
- Halving the minimum feature size results in quadrupling the maximum array size.
- The random average defect density remains constant for all technology nodes (from SIA roadmap).
- The defect density is not constant over the whole wafer and follows a gamma distribution.
- All metal connections between logic blocks are regularly shaped (i.e. straight and parallel) and regularly distanced.
- Defects are not closely packed (This follows from SIA prediction of cluster parameter = 2). This justifies the assumption that 1 extra column can tolerate 1 fault.
- Defects are circular, with diameter x.
- Defect size distribution follows an inverse power law shape $1/x^3$.
- To cause an open fault, two sections of metal have to be completely detached.
- A short is caused by any amount of extra material joining two adjacent lines.
- The die yield is the product of the individual layer yields.
- Vias and contacts are only present in the regions directly above the switch matrices.
- Width of lines and space between lines have identical size as given by the metal line pitch in the SIA roadmap.
- Lower metal layers are used for shorter, faster lines.
- Wafers are 12in in diameter.

6.1 Different metal layers on a single die

The SIA roadmap classifies interconnect layers into three types: metal 1, intermediate and global, each with different characteristics (Figure 5). Figure 6 shows the predicted yields of when each of three interconnect layers is considered separately. As can be seen, metal 1 layer, which is the lowest layer of interconnect, causes higher yield loss than the other layers. The lowest metal layer is used for short, fast metal interconnects. Being smaller and closer to the source and sink, these lines are the most used, and also are most susceptible to defects. It follows that a fault tolerant scheme targeting these lines exclusively will increase the yield of a wafer considerably. The maximum FPGA array size shown on the graph is assumed to be 120 X 120 CLBs, which is estimated from the size of Xilinx's XC2VP125 device manufactured in this technology.

6.2 More advanced technology nodes

The continuous development of wafer fabrication techniques means that interconnect characteristics will keep on evolving in the future. Driven by the need for higher density, metal lines will get smaller, thinner and, as a consequence, more susceptible to spot defects.

Figure 7 shows the predicted yield of the metal 1 layer for the technology nodes given in Table 1. The graph also highlights the maximum predicted array size (M) for each technology node. The yield loss is relatively well contained for the 130 and 90nm nodes. However, drastic losses appear at 45nm and 22nm. The yield loss due to metal 1 alone for the maximum array size in 22nm is predicted to be over 80%.

Figure 8 shows the total expected yield loss due to interconnect defects on all layers. Yield of around 40% for the biggest devices is predicted for the 90nm process technology. This value will certainly decrease if defects in the logic layers are considered. Predicted yield due to all interconnect defects for the 22nm node is close to 0%. Some form of fault tolerant scheme must therefore be introduced in order to produce any usable devices.

6.3 Improving yield with hardware redundancy

Because of the regular architecture of FPGAs, hardware

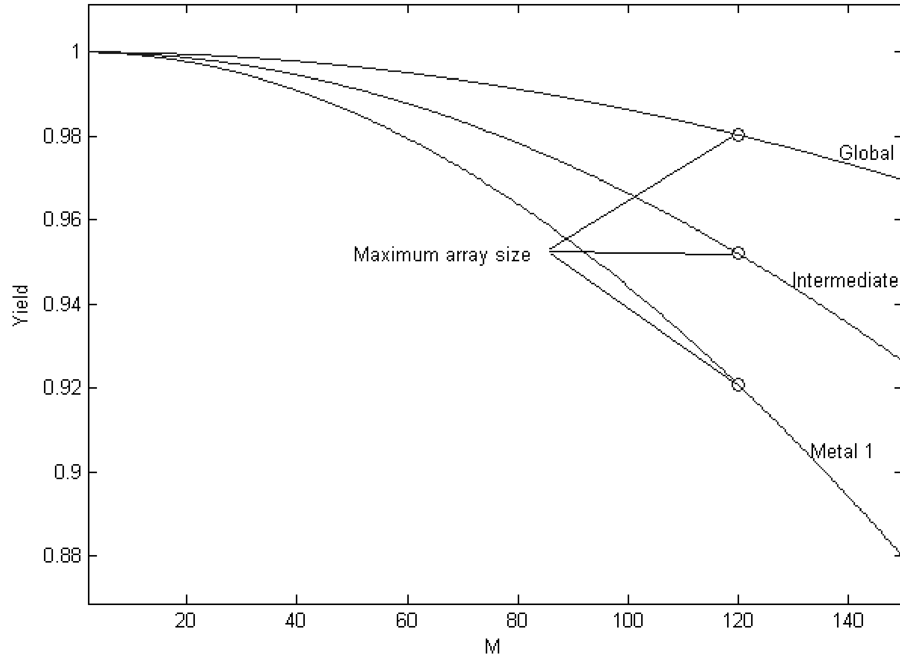

Figure 6: Yield comparison of different metal layers for the 130nm technology node

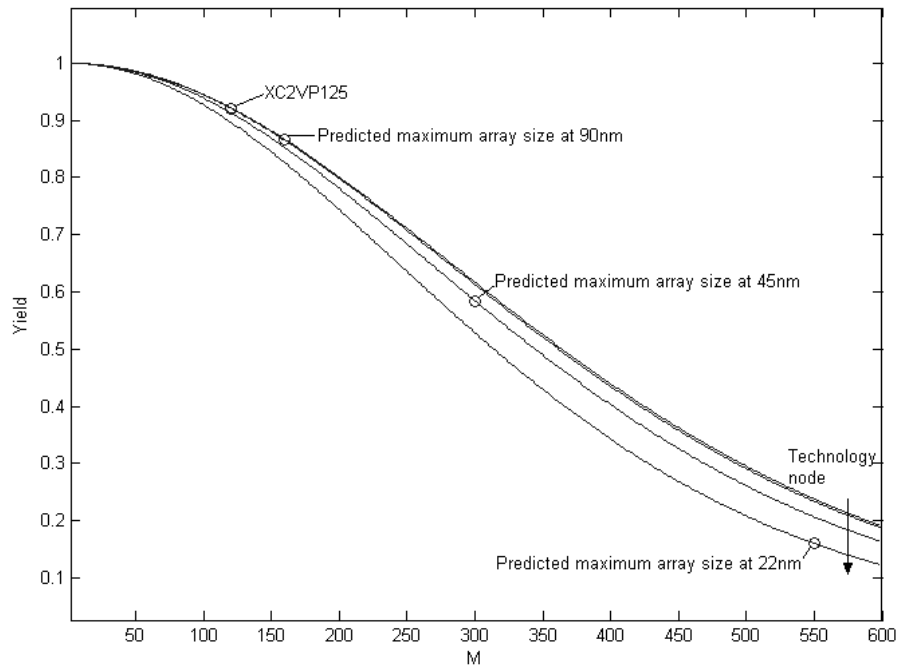

Figure 7: Metal 1 interconnect layer yield comparison for different technology nodes

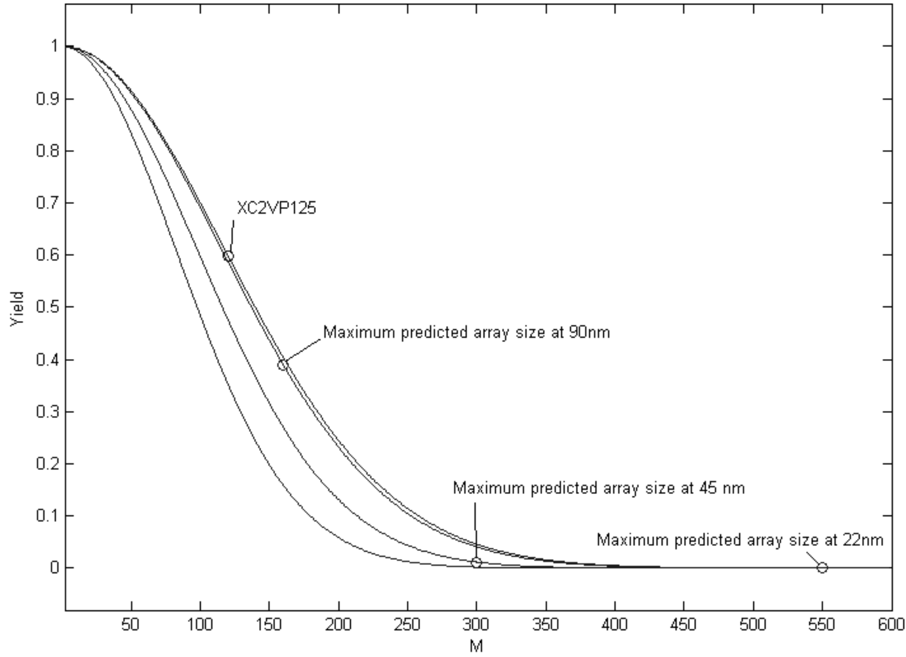

Figure 8: Overall die yield due to interconnect defects

redundancy is easy to introduce at the silicon design level. Usually a whole extra row or column is introduced, and this can be used as replacement for a row or column with defect. Since the SIA Roadmap indicates that spot defects are generally not clustered together (Cluster parameter = 2), we assume the worst case scenario that each defect requires a separate redundant row or column to be substituted. This technique however introduces other issues such as fault detection and location, timing effects and method of substitution. These issues are not dealt with in this study, the aim of which is to simply provide an account of the situation from the point of view of manufacturing yield.

Consider the case of 1-redundant circuit (i.e. a circuit with one redundant row/column) which can tolerate a single fault. The effective yield is the sum of the yield for dies with zero or one defect. Figure 9 shows the different yields caused by defects in metal 1 layer with and without one redundant column in the 90nm technology. It can be observed that, for array sizes comparable to the predicted maximum value, a yield improvement from 86% to nearly 100% is predicted if one fault can be tolerated. Figure 10 shows the same prediction but for the 22nm process node, where the yield is expected to improve from just under 20% to nearly 50%.

Adding hardware redundancy can improve the yield but comes at an increase in silicon area. Figure 11 shows how adding extra area can improve yield. The number of faults that can be tolerated increases with additional redundant circuits. It is possible that any given number of faults will only require a smaller number of extra rows or columns, if they happen to be close together on the silicon. However, under the worst case scenario when defects are widely scattered, n redundant rows or columns are required to tolerate n faults. At the 90nm node, most devices will only exhibit a limited number of fault, which implies that adding more than a certain amount of extra area will not result in any further improvement. This is shown in Figure 11; the yield rises rapidly to full scale for relatively small amount of extra silicon area. At 22nm, each device will exhibit multiple faults, and it can be observed how varying amounts of added silicon area can produce different amounts of yield improvements, up to the full wafer yield.

Another way to view the advantages of adding redundancy to improve yield is to calculate the total number of usable dies that result from the fabrication of a single wafer. The number of total dies that can fit in a wafer is obtained using (11), from [3]:

$$N(H,W) = \frac{\pi {R_e}^2}{HW} e^{-\frac{H}{R_e}} \tag{11}$$

where R_e is the wafer radius, and H and W are the dimensions of the chip. The number of good dies available from a wafer then becomes the product of the yield and the total number of fabricated dies.

Figure 12 shows how the number of good dies varies against increasing array size for the 90nm technology node. Figure 13 shows how the number of good dies per wafer varies as more faults are to be tolerated for future technology nodes. It is important to note how the 45nm curve reaches a peak and then drops as extra area is added to tolerate more faults. This is due to the little yield improvement obtained by adding a significant amount of extra area. The drop does not however imply that full yield is achieved. Simply, the advantage of being able to tolerate more faults comes at the price of less dies being fitted on the wafer.

6.4 Improving yield with fault tolerant reconfiguration

FPGAs are inherently redundant. A typical design mapped

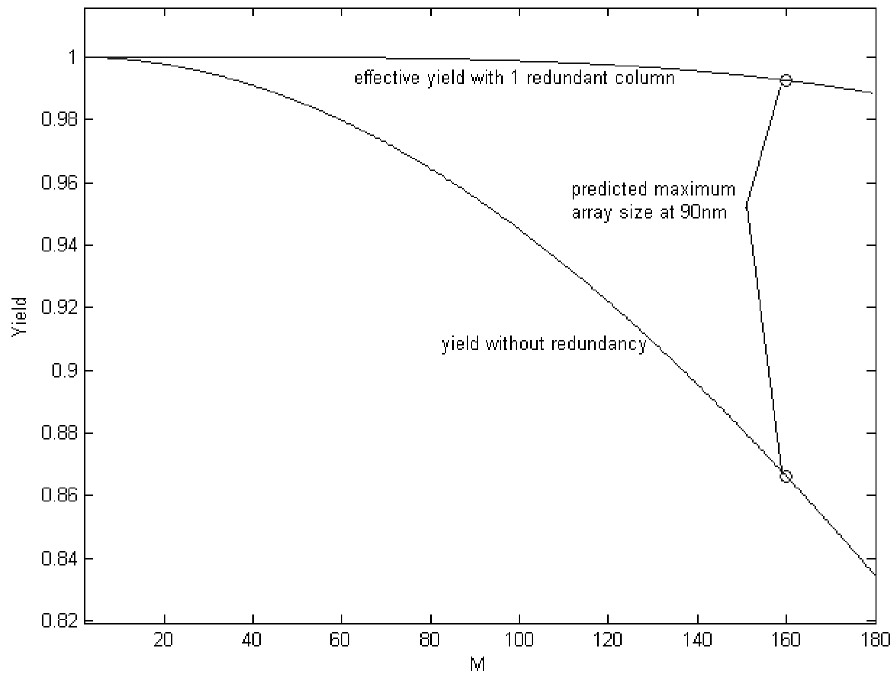

Figure 9: Metal 1 interconnect layer yield comparison with and without redundancy for the 90nm technology node

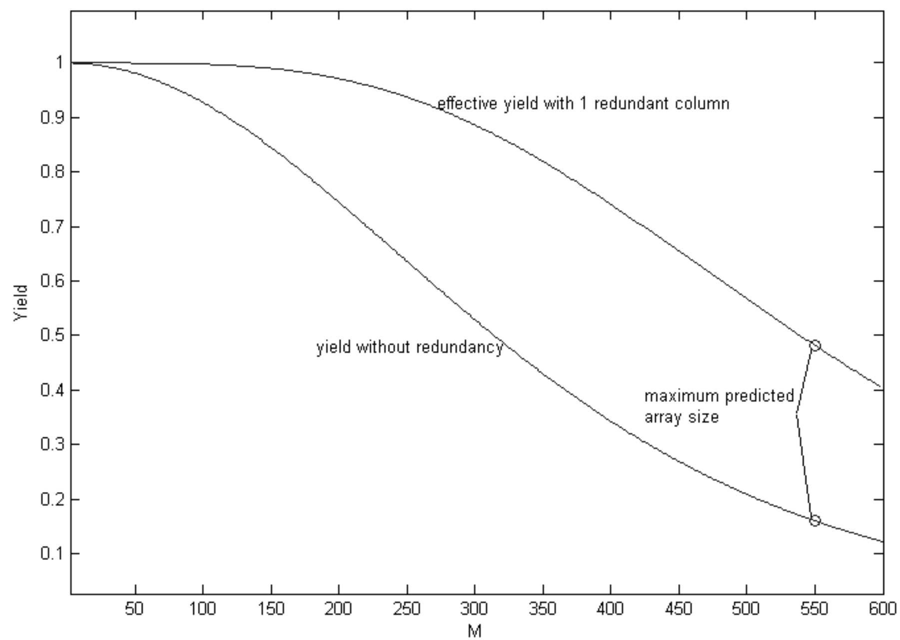

Figure 10: Metal 1 interconnect layer yield comparison with and without redundancy for the 22nm technology node

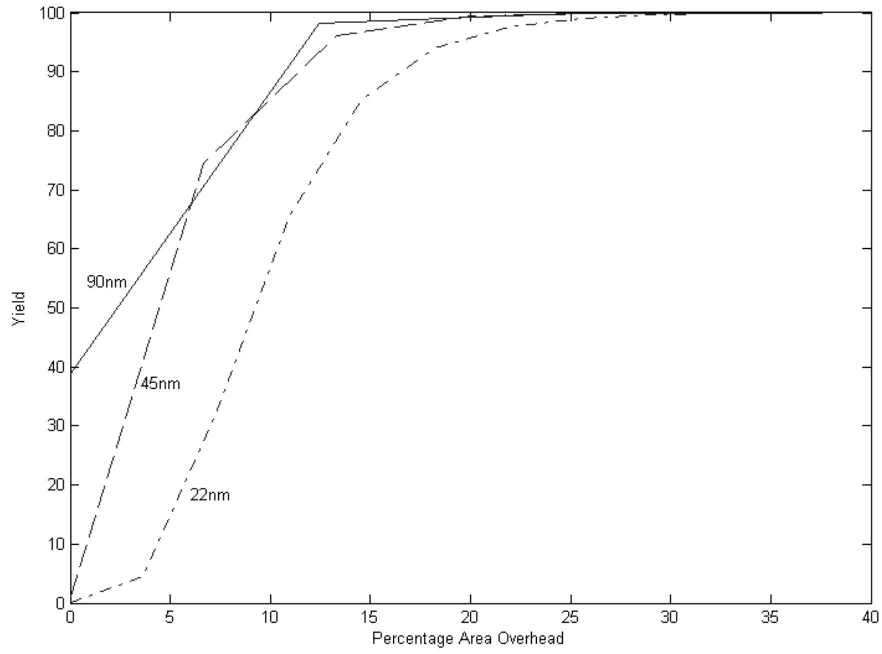

Figure 11: Yield improvement derived from added redundancy for the maximum predicted array sizes

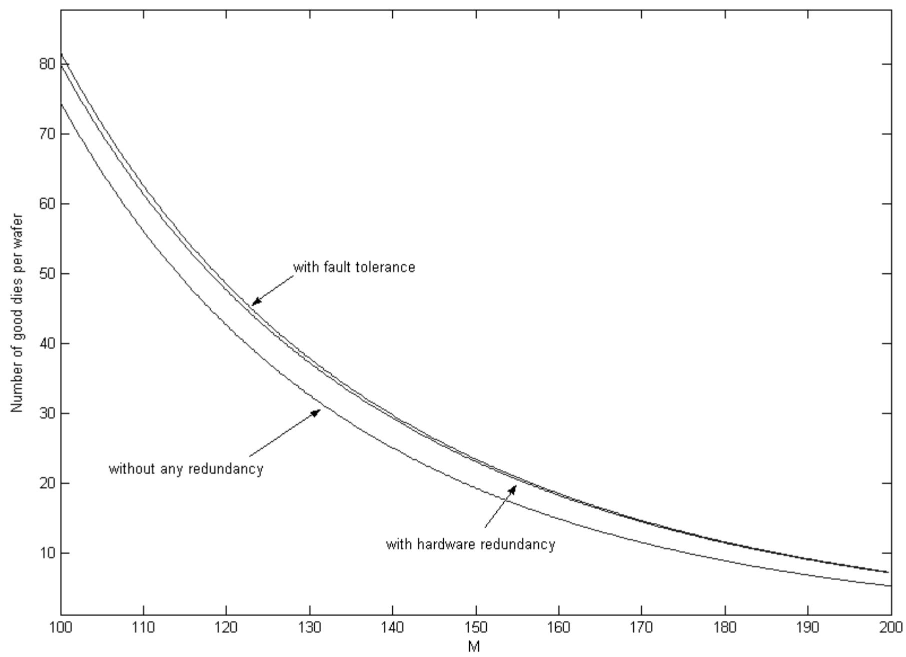

Figure 12: Number of good dies per 12 inch wafer as a function of array size for 90nm technology

onto a FPGA will, in general, not use all the resources on the device. It is therefore reasonable to consider the case where, employing a built-in self-test (BIST) strategy and suitable place-and-route algorithms, a method could be found to exploit the unused interconnect resources to replace any defects. For example, if an open fault exists on an interconnect line, it may be replaced by an unused track nearby. Again many issues remain to be resolved before such a scheme is viable, but these are outside the scope of the paper. For example, how can a defect be located and a suitable free resource that maintain timing integrity of the design be identified? However, it remains interesting to compare such a fault tolerant approach with that using redundant circuits from the perspective of yield improvement.

Figure 12 shows the number of usable dies from a 12 inch wafer obtained using a hardware redundancy scheme and a fault tolerance scheme. A fault tolerance scheme does not incur any area overhead. Therefore the number of good dies will always be larger when compared to a hardware redundancy scheme. The advantage of the fault tolerance scheme is clear for the smaller devices, where a redundant scheme incurs proportionally a higher area overhead. In contrast, a fault tolerance scheme costs no extra silicon area.

7. CONCLUSION

An analysis of the yield loss due to random defects in an FPGA die interconnect layers has been presented. Existing yield prediction methods have been adapted for the interconnect layers found on an FPGA die. Using the SIA predictions for future technology nodes, it has been possible to show how imperfection in the metal layers will contribute significantly to yield losses in the future. The analysis was restricted to random defects, which account for a significant portion of the yield loss.

This work has also shown how introducing redundancy can considerably improve manufacturing yield. Hardware redundancy incurs addition die area. The pros and cons of this method have been illustrated by calculating the total number of working dies obtained from a single wafer, which takes into account both the yield and the size of a die.

Finally, it has been demonstrated that a fault tolerance scheme can also offer significant improvements on yield at no extra area cost. Based on the observation that FPGAs are inherently redundant, the idea of a fault tolerance scheme is to accommodate the design on a FPGA device which may have defects, but contains unused interconnect resources.

The current results have not be verified against actual yield data from FPGA manufacturers. Further work will include such verification assuming that the necessary yield statistics can be obtained. Other works include exploring details of how to exploit the inherent spare resources on the FPGA to provide fault tolerance, suitable BIST methods to identify faults cheaply and quickly on FPGA and methods for replacing defective interconnects with the unused ones.

8. ACKNOWLEDGEMENTS

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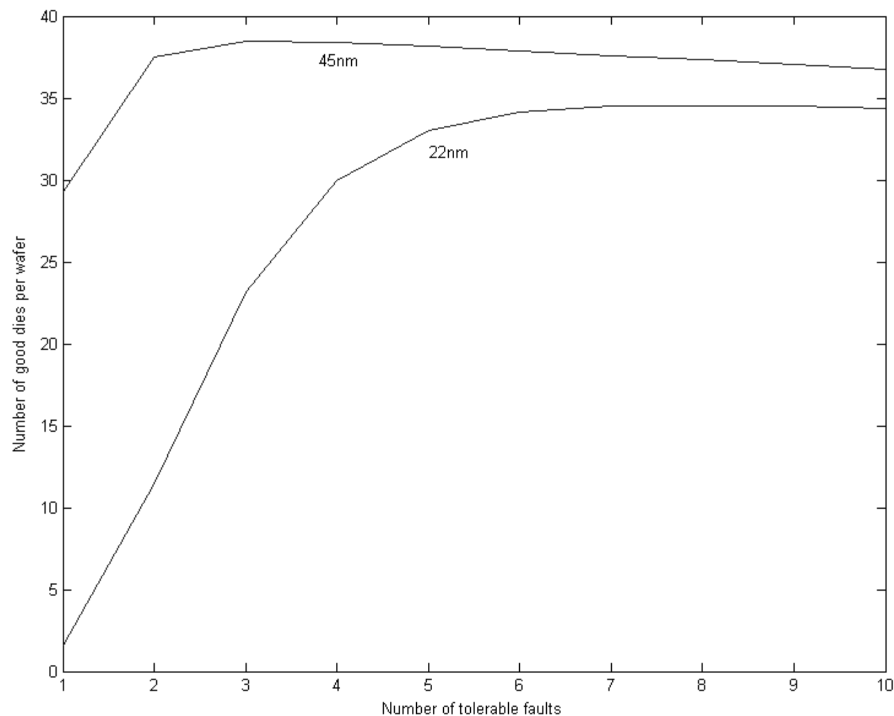

Figure 13: Number of good dies for 45 nm and 22nm technology nodes

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